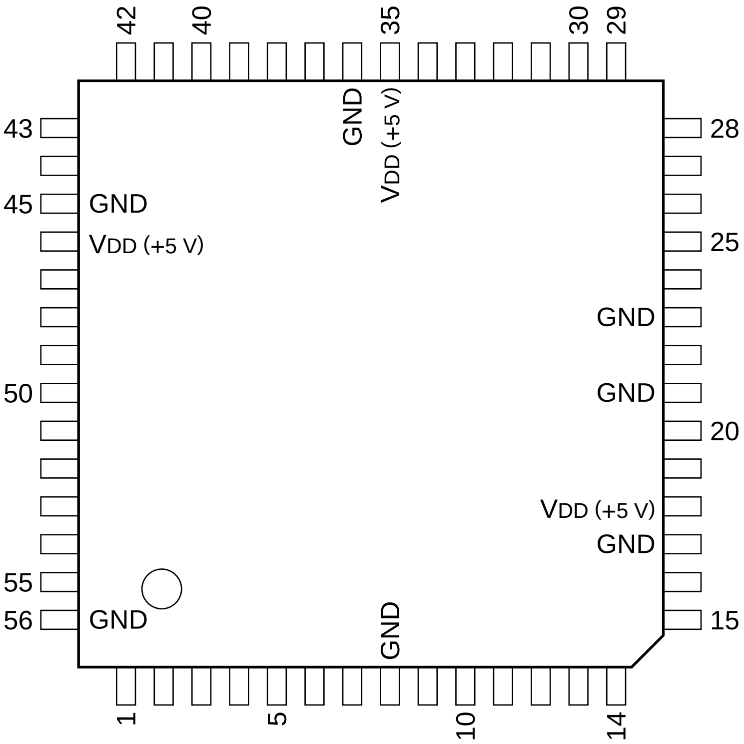
C-MOS IEEE 1284 PERIPHERAL CONTROLLER

—TOP VIEW—



(V_{DD} = +5 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	BPo$\overline{\text{INT2}}$	15	I/O	bD1	29	I	BPi$\overline{\text{DEND1}}$	43	I/O	BPbD1
2	O	BPo$\overline{\text{INT1}}$	16	I/O	bD0	30	I	BPi$\overline{\text{DAK0}}$	44	I/O	BPbD0
3	O	BPo$\overline{\text{INT0}}$	17	—	GND	31	O	BPo	45	—	GND
4	I	iA3	18	—	V_{DD}	32	O	BPo$\overline{\text{DEND0}}$	46	—	V_{DD}
5	I	iA2	19	I	i$\overline{\text{RD}}$/R$\overline{\text{W}}$	33	I	BPiCLS	47	I	BPi$\overline{\text{SEI}}$
6	I	iA1	20	I	i$\overline{\text{WR}}$/$\overline{\text{EN}}$	34	O	BPoRT	48	I	BPi$\overline{\text{AF}}$
7	I	iA0	21	—	GND	35	—	V_{DD}	49	I	BPi$\overline{\text{INI}}$
8	—	GND	22	I	BPiCLK	36	—	GND	50	I	BPi$\overline{\text{STB}}$
9	I/O	bD7	23	—	GND	37	I/O	BPbD7	51	O	BPoPE
10	I/O	bD6	24	I	i$\overline{\text{RST}}$	38	I/O	BPbD6	52	O	BPo$\overline{\text{ACK}}$
11	I/O	bD5	25	I	iCIS	39	I/O	BPbD5	53	O	BPoBY
12	I/O	bD4	26	I	i$\overline{\text{CS}}$	40	I/O	BPbD4	54	O	BPo$\overline{\text{FT}}$
13	I/O	bD3	27	I	BPi$\overline{\text{DAK1}}$	41	I/O	BPbD3	55	O	BPoSE
14	I/O	bD2	28	O	BPo$\overline{\text{DRQ1}}$	42	I/O	BPbD2	56	—	GND

INPUT

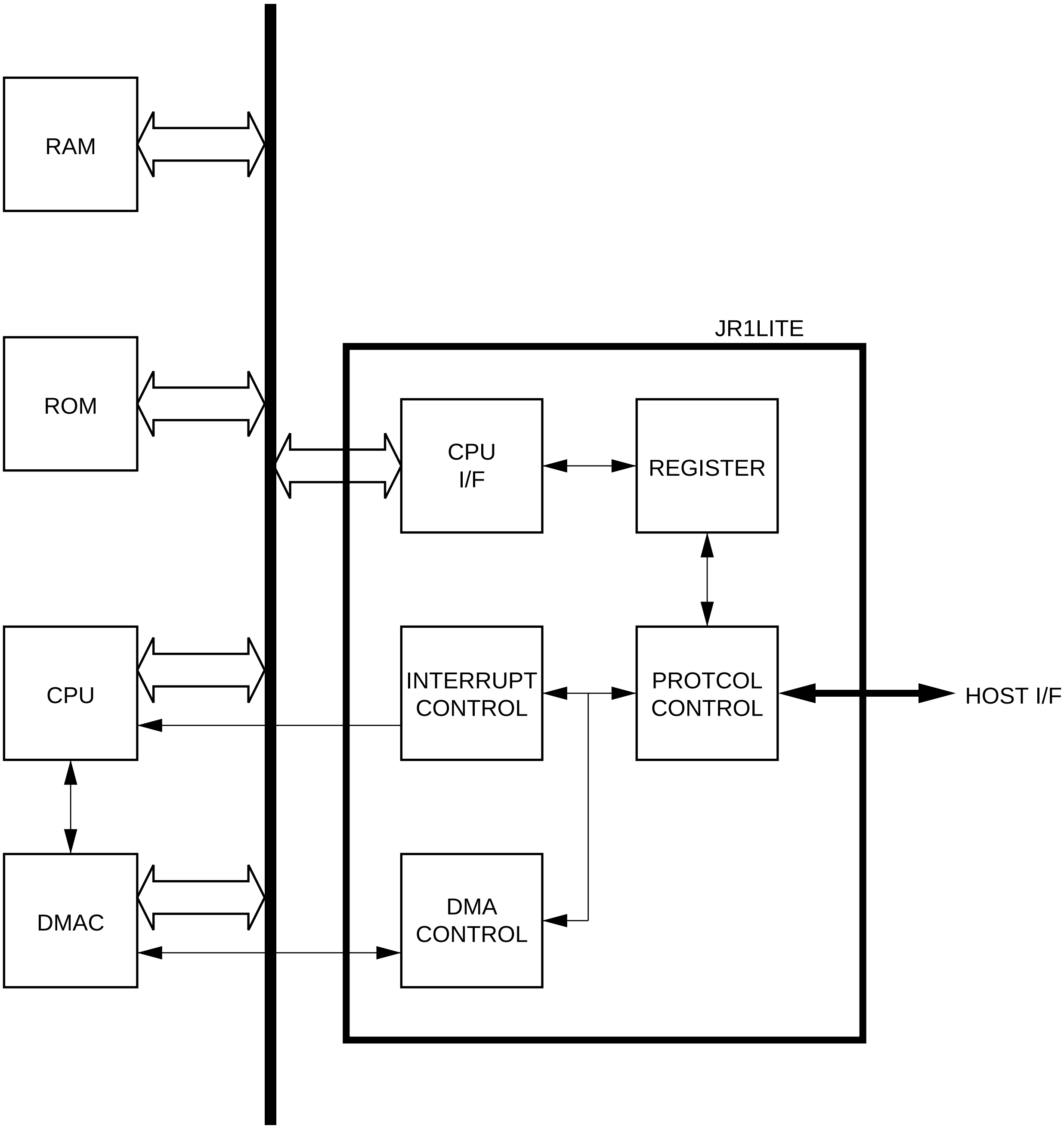
BPi$\overline{\text{AF}}$: COMPATIBILITY = n AUTO Fd
BPiCLK : CLOCK
BPiCLS : COMPATIBILITY MODE LEVEL SELECT
BPi$\overline{\text{DAK0}}$: DMA ACKNOWLEDGE0
BPi$\overline{\text{DAK1}}$: DMA ACKNOWLEDGE1
BPi$\overline{\text{DEND1}}$: DMA END1
BPi$\overline{\text{INI}}$: COMPATIBILITY = n INITIAL
BPi$\overline{\text{SEI}}$: COMPATIBILITY = n SELECT IN
BPi$\overline{\text{STB}}$: COMPATIBILITY = n STROBE
iA0 - iA3 : ADDRESS
iCIS : CPU INTERFACE SELECT
i$\overline{\text{CS}}$: CHIP SELECT
i$\overline{\text{RD}}$/W$\overline{\text{R}}$: READ/READ WRITE SELECT
i$\overline{\text{RST}}$: RESET
i$\overline{\text{WR}}$/$\overline{\text{EN}}$: WRITE/ENABLE

OUTPUT

BPo$\overline{\text{ACK}}$: COMPATIBILITY = n ACK
BPoBY : COMPATIBILITY = BUSY
BPo$\overline{\text{DEND0}}$: DMA END0
BPo$\overline{\text{DRQ0}}$: DMA REQUEST0
BPo$\overline{\text{DRQ1}}$: DMA REQUEST1
BPo$\overline{\text{FT}}$: COMPATIBILITY = n FAULT
BPo$\overline{\text{INT0}}$: INTERRUPT REQUEST0
BPo$\overline{\text{INT1}}$: INTERRUPT REQUEST1
BPo$\overline{\text{INT2}}$: INTERRUPT REQUEST2
BPoPE : COMPATIBILITY = P ERROR
BPoRT : INDICATE REVERSE TRANSFER
BPoSE : COMPATIBILITY = SELECT

INPUT/OUTPUT

bD0 - bD7 : DATA BUS
BPbD0 - BPbD7 : COMPATIBILITY = DATA


RAM
ROM
JR1LITE
CPU
I/F
REGISTER
CPU
INTERRUPT
CONTROL
PROTCOL
CONTROL
HOST I/F
DMAC
DMA
CONTROL