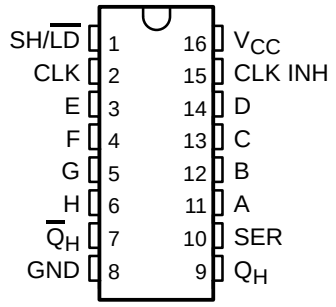
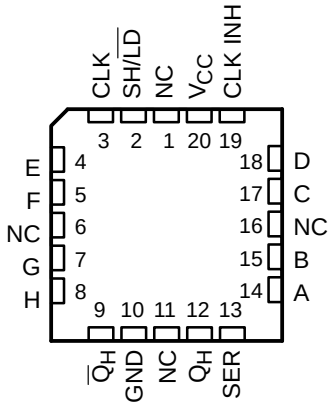
SCLS371 – MAY 1997

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC165 . . . J OR W PACKAGE
SN74AHC165 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC165 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’AHC165 are 8-bit parallel-load shift registers that, when clocked, shift the data toward a serial (Q_H) output. Parallel-in access to each stage is provided by eight individual direct data (A–H) inputs that are enabled by a low level at the shift/load (SH/$\overline{LD}$) input. The ’AHC165 also feature a clock-inhibit (CLK INH) function and a complementary serial ($\overline{Q}_H$) output.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. While SH/$\overline{LD}$ is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

The SN54AHC165 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC165 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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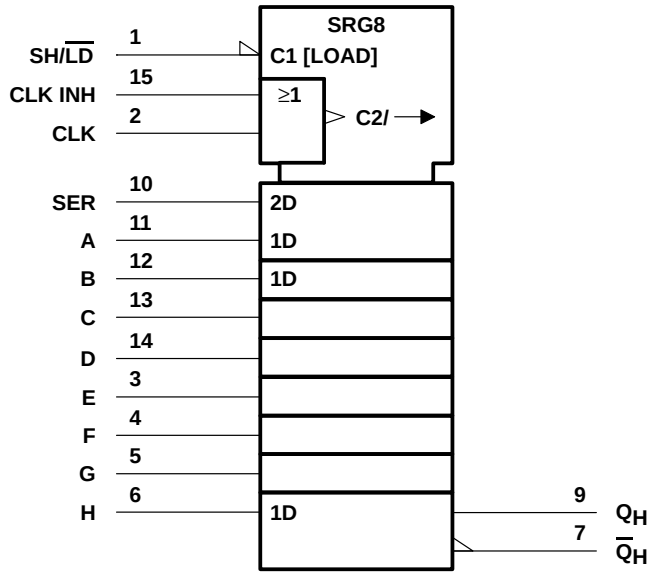
FUNCTION TABLE

INPUTS			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	L	↑	Shift†
H	↑	L	Shift†

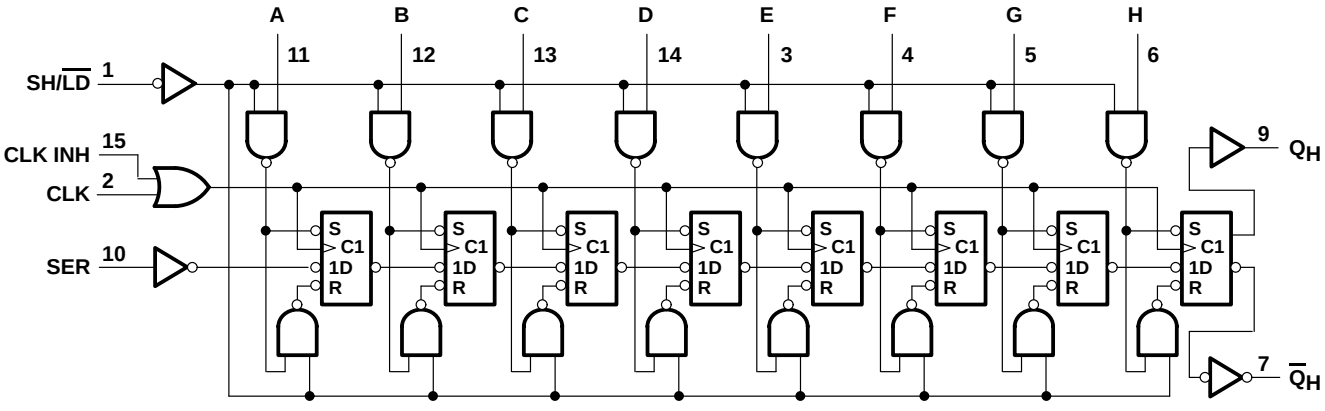
† Shift = content of each internal register shifts toward serial output Q_H. Data at SER is shifted into the first register.

logic symbol†



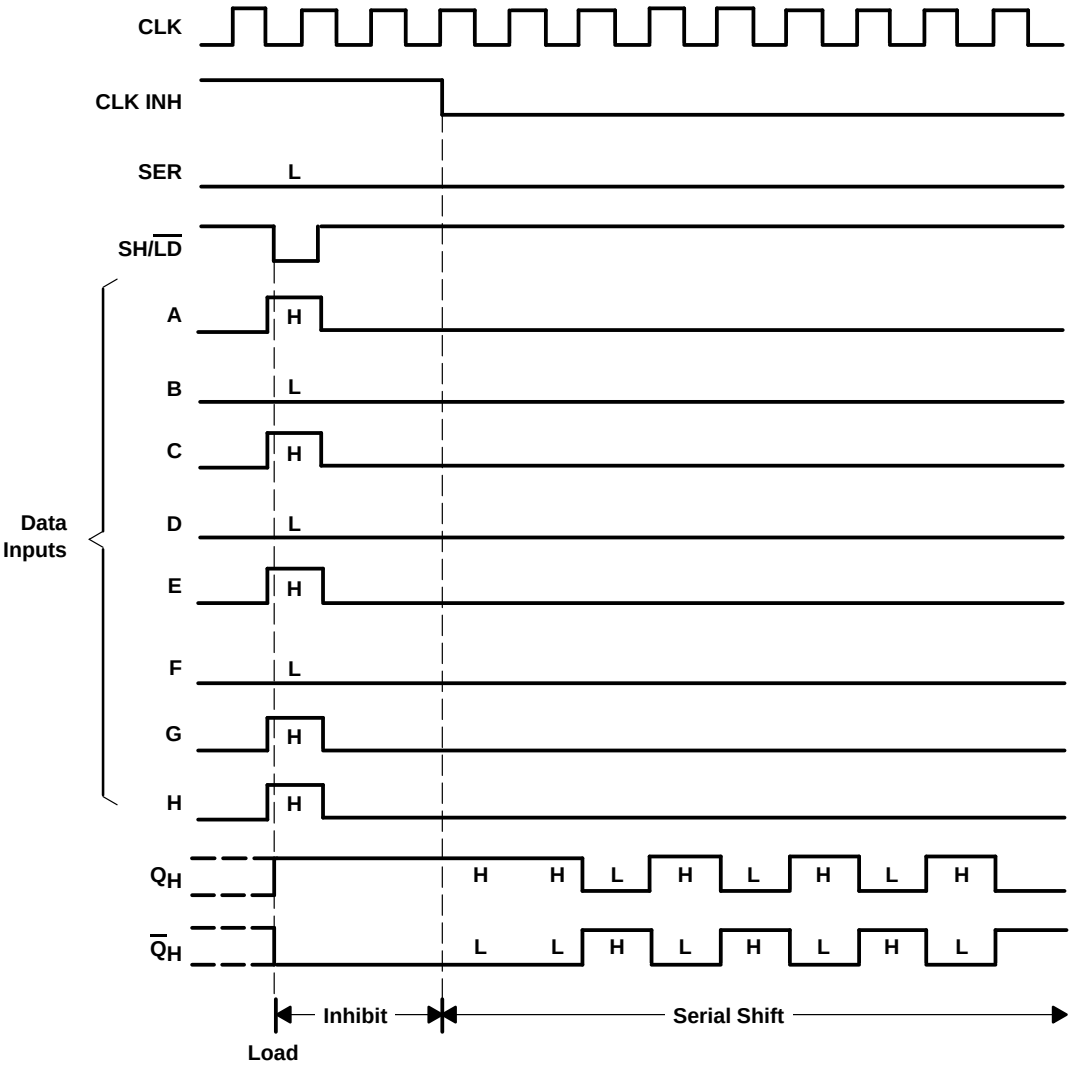
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

typical shift, load, and inhibit sequence



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 113°C/W
DB package . . . . . 131°C/W
N package . . . . . 78°C/W
PW package . . . . . 149°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

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recommended operating conditions (see Note 3)

			SN54AHC165		SN74AHC165		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	– 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC165		SN74AHC165		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10				10	pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54AHC165		SN74AHC165		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low							ns
		SH/$\overline{LD}$ low							
t_{su}	Setup time	CLK INH high before CLK↑							ns
		CLK INH low before CLK↑							
		Data before SH/$\overline{LD}$↓							
		SER before CLK↑							
		SH/$\overline{LD}$ high before CLK↑							
t_h	Hold time	SER data after CLK↑							ns
		PAR data after SH/$\overline{LD}$↓							

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54AHC165		SN74AHC165		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low							ns
		SH/$\overline{LD}$ low							
t_{su}	Setup time	CLK INH high before CLK↑							ns
		CLK INH low before CLK↑							
		Data before SH/$\overline{LD}$↓							
		SER before CLK↑							
		SH/$\overline{LD}$ high before CLK↑							
t_h	Hold time	SER data after CLK↑							ns
		PAR data after SH/$\overline{LD}$↓							

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC165				UNIT
				T_A = 25°C			MIN MAX	
				MIN	TYP	MAX		
f_{max}			C_L = 15 pF*					MHz
			C_L = 50 pF					
t_{PLH}*	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$	C_L = 15 pF					ns
t_{PHL}*								
t_{PLH}*	CLK	Q_H or $\overline{Q}_H$	C_L = 15 pF					ns
t_{PHL}*								
t_{PLH}*	H	Q_H or $\overline{Q}_H$	C_L = 15 pF					ns
t_{PHL}*								
t_{PLH}	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$	C_L = 50 pF					ns
t_{PHL}								
t_{PLH}	CLK	Q_H or $\overline{Q}_H$	C_L = 50 pF					ns
t_{PHL}								
t_{PLH}	H	Q_H or $\overline{Q}_H$	C_L = 50 pF					ns
t_{PHL}								

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC165				UNIT
				T_A = 25°C			MIN MAX	
				MIN	TYP	MAX		
f_{max}			C_L = 15 pF					MHz
			C_L = 50 pF					
t_{PLH}	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$	C_L = 15 pF					ns
t_{PHL}								
t_{PLH}	CLK	Q_H or $\overline{Q}_H$	C_L = 15 pF					ns
t_{PHL}								
t_{PLH}	H	Q_H or $\overline{Q}_H$	C_L = 15 pF					ns
t_{PHL}								
t_{PLH}	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$	C_L = 50 pF					ns
t_{PHL}								
t_{PLH}	CLK	Q_H or $\overline{Q}_H$	C_L = 50 pF					ns
t_{PHL}								
t_{PLH}	H	Q_H or $\overline{Q}_H$	C_L = 50 pF					ns
t_{PHL}								

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC165					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF						MHz
			C_L = 50 pF						
t_{PLH}*	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$	C_L = 15 pF						ns
t_{PHL}*									
t_{PLH}*	CLK	Q_H or $\overline{Q}_H$	C_L = 15 pF						ns
t_{PHL}*									
t_{PLH}*	H	Q_H or $\overline{Q}_H$	C_L = 15 pF						ns
t_{PHL}*									
t_{PLH}	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$	C_L = 50 pF						ns
t_{PHL}									
t_{PLH}	CLK	Q_H or $\overline{Q}_H$	C_L = 50 pF						ns
t_{PHL}									
t_{PLH}	H	Q_H or $\overline{Q}_H$	C_L = 50 pF						ns
t_{PHL}									

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC165					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF						MHz
			C_L = 50 pF						
t_{PLH}	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$	C_L = 15 pF						ns
t_{PHL}									
t_{PLH}	CLK	Q_H or $\overline{Q}_H$	C_L = 15 pF						ns
t_{PHL}									
t_{PLH}	H	Q_H or $\overline{Q}_H$	C_L = 15 pF						ns
t_{PHL}									
t_{PLH}	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$	C_L = 50 pF						ns
t_{PHL}									
t_{PLH}	CLK	Q_H or $\overline{Q}_H$	C_L = 50 pF						ns
t_{PHL}									
t_{PLH}	H	Q_H or $\overline{Q}_H$	C_L = 50 pF						ns
t_{PHL}									

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noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		SN74AHC165			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.4	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz		pF

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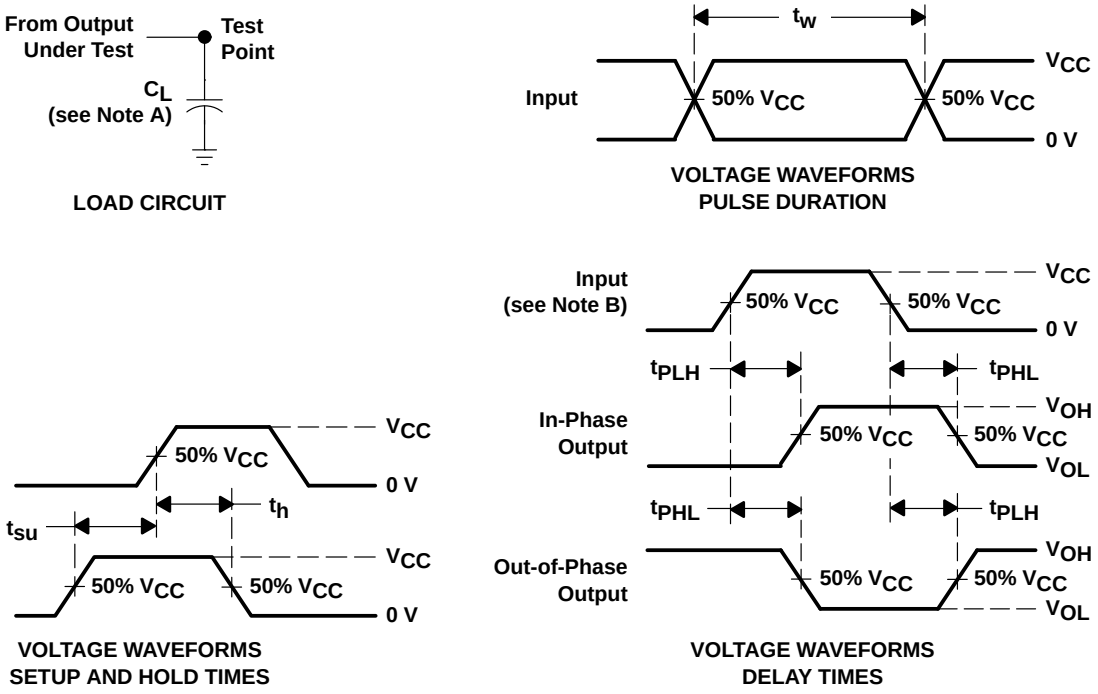
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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