

APPLICATION NOTE

ABSTRACT

The SA9500/SA9502 is a front-end receive downconverter designed for a CDMA/AMPS phone application. It consists of three individual mixers: 1900 MHz PCS CDMA, 800 MHz cellular CDMA, and 800 MHz cellular FM, which can downconvert these RF frequency bands to 50–300 MHz IF based upon the application. All the mixers are designed to meet the stringent spurious rejection requirements in the cellular and PCS bands. Implemented in an advanced silicon BICMOS process, the SA9500 operates from 2.7V to 3.3V (2.7V to 4.0V for the SA9502) with very low current consumption and high linearity. It can also be powered down into sleep mode for power management. An on-chip LO buffer can provide the LO signal elsewhere in the radio.

AN2002

Application of the SA9500/SA9502 dual-band CDMA/AMPS downconverter

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1999 Feb 02

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1. INTRODUCTION

The SA9500/SA9502 is a front-end receive downconverter designed for a CDMA/AMPS phone application. It consists of three individual mixers: 1900 MHz PCS CDMA, 800 MHz cellular CDMA, and 800 MHz cellular FM, which can downconvert these RF frequency bands to 50–300 MHz IF based upon the application. All the mixers are designed to meet the stringent spurious rejection requirements in the cellular and PCS bands. Implemented in an advanced silicon BICMOS process, the SA9500 operates from 2.7V to 3.3V (2.7V to 4.0V for the SA9502) with very low current consumption and high linearity. It can also be powered down into sleep mode for power management. An on-chip LO buffer can provide the LO signal elsewhere in the radio.

2. APPLICATION OF THE SA9500/SA9502 IN CDMA/AMPS PHONE SYSTEM

Efficient band usage and low power consumption has resulted in the rapid growth of code division multiple access (CDMA) systems in cellular and PCS applications. To realize the benefits of CDMA technology, the high performance RF receive components must be selected to achieve low noise and high levels of linearity simultaneously with low current consumption. On the other hand, the traditional analog AMPS system still remains of interest to the service providers. The SA9500/SA9502 front-end down converters are designed to meet these demands by supporting both the cellular/PCS bands and CDMA/FM modes. Figure 1 is the block diagram of the typical receive path in a wireless phone system and shows where the SA9500/SA9502 will fit in the receive front-end.

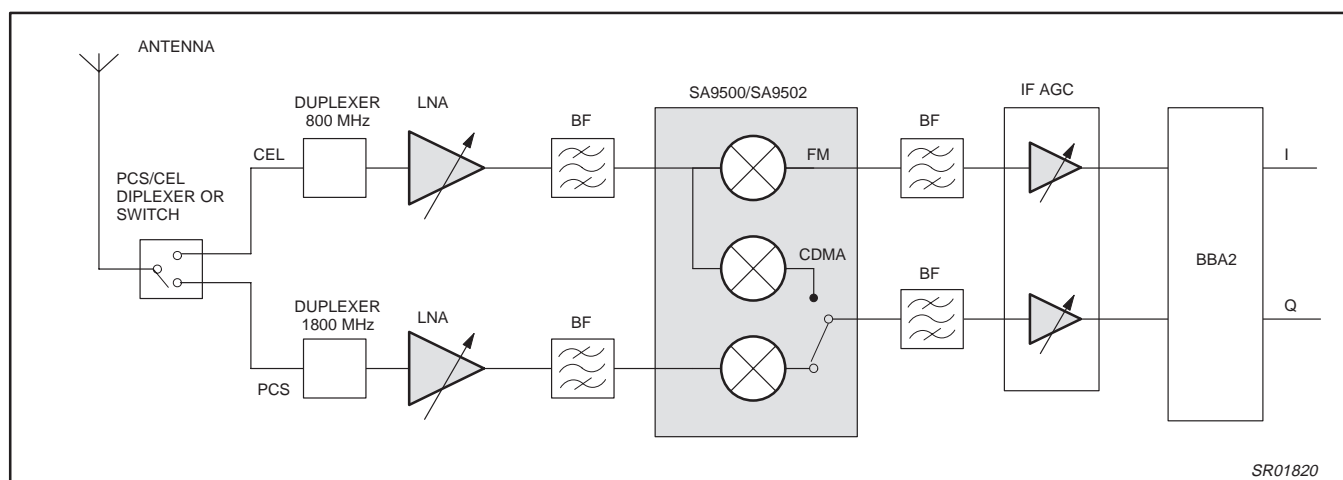


Figure 1. Block Diagram of Rx Path of a Wireless Phone System

Compared with traditional passive mixers, the SA9500/SA9502 requires much lower gain from the LNA in front of it because it has 7dB of conversion gain in cellular FM mode and around 11dB in cellular CDMA and PCS modes, instead of a loss from passive mixers. Although passive mixers can usually provide better linearity, the LO drive power needs to be much higher (about +7dBm) than in the SA9500/SA9502 (about -3dBm), hence the power consumption is much higher. So the SA9500/SA9502 can yield much better performance than a passive down converter with similar power consumption.

3. APPLICATION BOARD

The schematic of the SA9500/SA9502 application board is shown in Figure 11 on page 14. In the SA9500/SA9502, there are two input ports (Cellular and PCS), two differential IF outputs (CDMA and FM), as well as LO input and LO output ports. The S-parameters of all these ports are provided in the Datasheet. All of these ports are matched to 50 Ω single-ended source or load on the application board. Some of the matching schemes used are described below.

Application of the SA9500/SA9502 dual-band CDMA/AMPS downconverter

AN2002

3.1 Balun circuit

The balun circuit used in the PCS RF input port converts the single-ended PCS RF input signal to a differential input signal to improve the IP2 of the mixer and matches the 50 Ω source to the input impedance of the SA9500/SA9502. The standard configuration of the balun circuit is depicted in Figure 2.

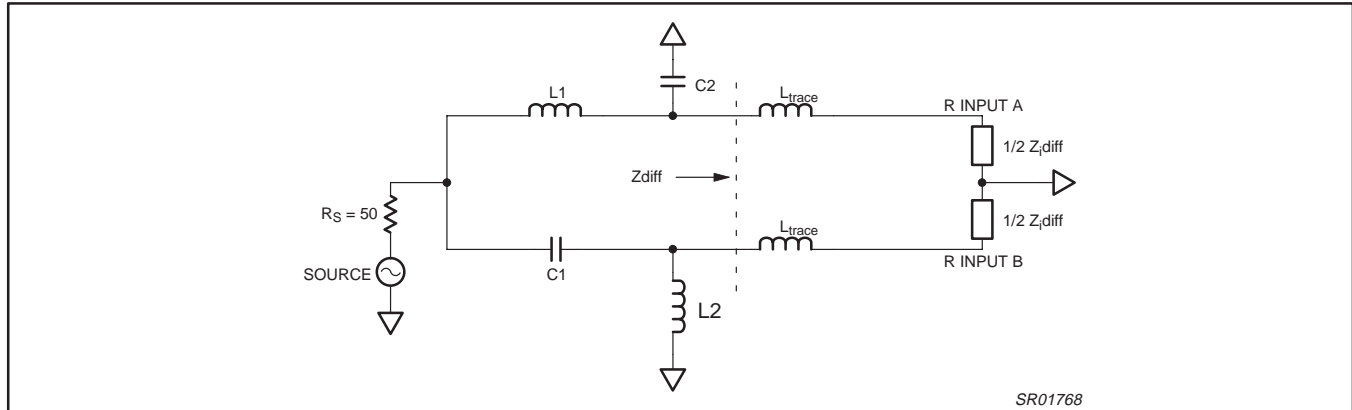


Figure 2. Balun Circuit

In a simplified situation of matching to a real load, assuming the single-ended signal source resistance is R_S and the differential load resistance is R_{diff} , $C_1 = C_2 = C$ and $L_1 = L_2 = L$, then,

$$L = \frac{\sqrt{R_S \times R_{diff}}}{2 \times \pi \times f} \quad \text{Eq. 1}$$

$$C = \frac{1}{2 \times \pi \times f \times \sqrt{R_S \times R_{diff}}} \quad \text{Eq. 2}$$

On the SA9500/SA9502 application board, the trace between the IC pins and the matching circuit is 120mil in length and 14mil in width on 62 mil thick FR4 board which produces approximately 2.5nH of trace inductance (L_{trace}). The impedance looking into the IC from the balun can be obtained by a simple transformation. For the SA9500/SA9502 application board at 1.9GHz, $R_{diff} = 32 \Omega$ and $X_{diff} = -4 \Omega$. The small reactance can be absorbed into the matching network experimentally. So treating the load as real, Eq.1 and Eq. 2 calculated at 1.9GHz produced $L = 3.3\text{nH}$ and $C = 2.0\text{pF}$. These results were used as starting values on the application board. Further optimization on the bench to adjust for additional parasitic effects and component variations led to the actual values $L_7 = L_9 = 4.7\text{nH}$ and $C_{17} = C_{19} = 1.5\text{pF}$, which yielded a return loss better than 12dB. Capacitors C16, C18 and C22 on the application board are for DC blocking and RF coupling. To keep the bench optimization manageable, it is suggested that all four components be changed together according to Eq. 1 and Eq. 2. For more details about the balun circuit, please refer to section 4.3 of Philips Semiconductors application note AN96106.

Application of the SA9500/SA9502 dual-band CDMA/AMPS downconverter

AN2002

3.2 Current combiner circuit

The IF outputs of the SA9500/SA9502 for both the CDMA and FM mixers are open-collector differential. It is possible to implement a current combiner or a balanced transformer to convert the differential signal to single-ended while achieving an impedance match at the same time. On the application board, a current combiner is used for the cellular FM IF output, while a balanced transformer is used for the cellular CDMA and PCS IF outputs. The typical current combiner shown in Figure 3 is composed of two sections: the current combining circuit and the impedance matching network. The current combining circuit, consisting of C1, C2, and L1, transforms the two differential currents from IFA and IFB into two in-phase currents while the matching network made up of R1, C4, and L2, brings the output to the desired impedance to match to the load. When tuning the current combiner, the recommended procedure involves two steps:

1. Disconnect the matching network and tune the combining circuit until it resonates at the desired IF frequency at which point the output impedance is purely resistive, i.e., the reactance is zero. The resistance is dominated by the parasitic resistance of L1 and R1.
2. Connect the matching network and adjust the component values to get the desired output impedance (50 Ω for the application board).

As a starting point for the current combiner circuit, C1 plus C_{OUT} with half of L1 should resonate at the desired frequency, and C2 plus C_{OUT} with 1/2 of L1 also should resonate at the desired frequency. More details on the current combiner circuit can be found in Philips Semiconductors application note AN1777.

For the CDMA IF output port, a balanced transformer, which has a 1:8 impedance ratio, is utilized to achieve the balun function. To match to a 50 Ω load, each side of the primary side of the transformer needs to be 200 Ω to ground which is realized by the matching components, R3, C7, C20, and L4 for side A, and R2, C8, C21, and L5 for side B (refer to Figure 11). All other matching circuits are simple L or T networks, and are quite straight forward.

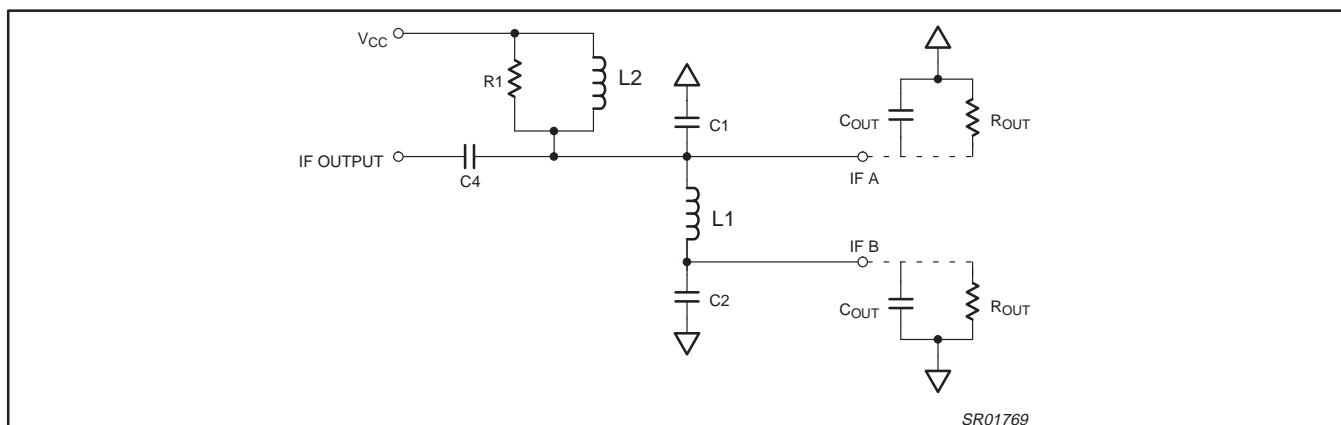


Figure 3. Current Combiner

Application of the SA9500/SA9502 dual-band CDMA/AMPS downconverter

AN2002

4. PARTS LIST AND ASSEMBLY

The parts list and layout for the SA9500/SA9502 application board are presented in Table 9 and Figure 12, respectively. The parts list is based on the match at an IF of 85.4MHz for the cellular FM and CDMA IF outputs. If the PCS 210 MHz IF is used, the appropriate component values are $L4=L5=27\text{nH}$, $C20=C21=5.6\text{pF}$. The Mini-Circuit transformer L10 has 8:1 impedance ratio with 0.7 dB insertion loss at 85 MHz and 1.0 dB at 210MHz. Measuring the insertion loss of this balanced to unbalanced transformer is easily accomplished by putting two of them back to back, i.e., from unbalanced to balanced and then from balanced to unbalanced, and measure the loss, half of which is the insertion loss. Also be careful of the orientation of this part when loaded onto the board. The two-lead side faces the CDMA output SMA connector, and the three-lead side faces the IC. For the SA9500/SA9502, there is a slightly larger pad close to C1 on the application board which identifies Pin 1. Solder the part carefully as it is easy to get a solder bridge between pins. All other components are standard resistors, capacitors, inductors, and connectors that should pose no special problems. The SA9502 should be used if direct PCS LO input is desired.

5. MEASUREMENTS AND RESULTS

Before performing measurements, the mode of operation must be properly set by adjusting the two mode setting jumpers according to Table 1 for the SA9500 and Table 2 for the SA9502. Basically, there are two differences between the SA9500 and the SA9502. First, the PCS LO input of the SA9500 injected at the CEL LO IN Pin16 is always fed through the doubler and the LO buffer output can be selected with either direct LO output or doubled output. The PCS LO input of the SA9502 can be selected either direct LO input mode in which PCS LO is injected at the PCS LO IN Pin 14 or doubled LO input mode in which PCS LO is injected at the CEL LO IN Pin 16 with the LO buffer output at 2GHz in both modes. Second, the PCS mixer is designed for high-side LO injection for the SA9500 and for low-side LO injection for the SA9502. The test conditions and results for some important measurements used in the characterization of the SA9500/SA9502 are as follows.

Table 1. Mode Selection Summary of the SA9500

PCS/CEL (Pin 6)	CDMA/FM/LO doubler (Pin 17)	Mode
low	low	Cellular FM
low	high	Cellular CDMA
high	low	CDMA PCS, 1GHz (LO out)
high	high	CDMA PCS, 2GHz (2xLO out)

Table 2. Mode Selection Summary of the SA9502

PCS/CEL (Pin 6)	CDMA/FM/LO doubler (Pin 17)	Mode
low	low	Cellular FM
low	high	Cellular CDMA
high	low	CDMA PCS, direct LO in
high	high	CDMA PCS, LO via frequency doubler

Application of the SA9500/SA9502 dual-band CDMA/AMPS downconverter

AN2002

5.1 IP3

IP3 measurements were accomplished using two tone RF signals into the RF port. The two tone signals are 60KHz apart in frequency at a power level of -23dBm for FM mode, and 900KHz apart at a power level of -30dBm for CDMA mode. The -3dBm LO power was used for this test.

The results of the IP3 measurement in cellular FM mode is presented in Figure 4 which was taken from an HP 8594E Spectrum Analyzer. $\text{IIP3} = \text{PRF}(\text{input}) + 1/2\Delta = +8.8\text{dBm}$, where Δ is the difference between the fundamental output power and the intermod power.

The IP3 performance vs LO drive level is shown in Figure 5.

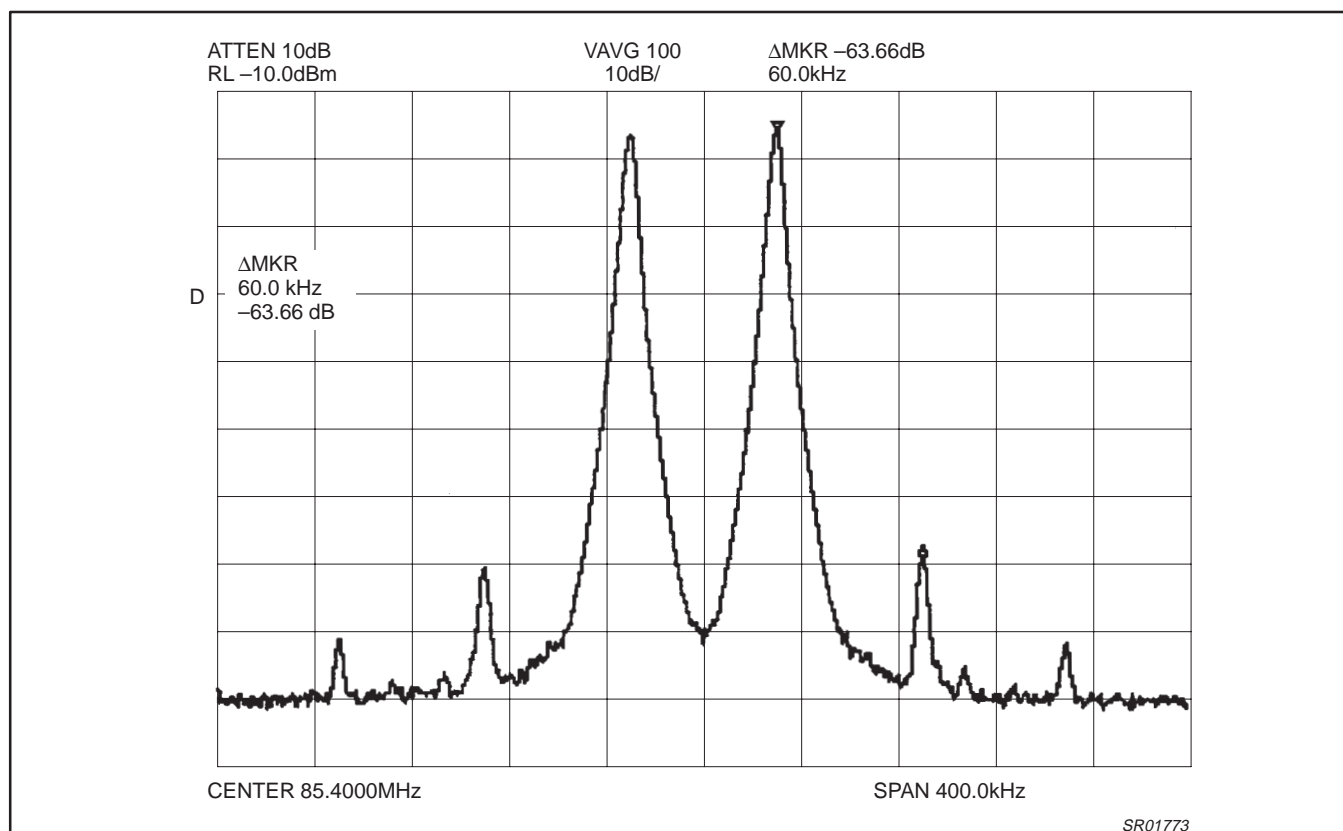


Figure 4. IP3 measurement for Cellular FM mode
RF input power = -23dBm

Application of the SA9500/SA9502 dual-band CDMA/AMPS downconverter

AN2002

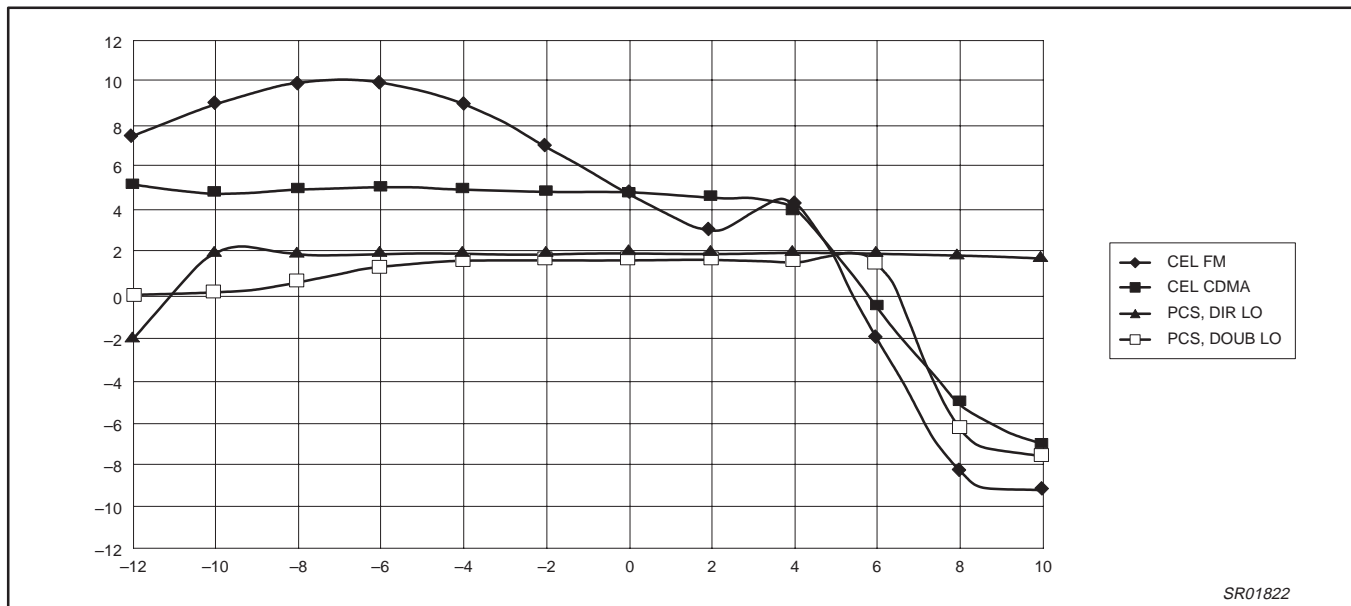


Figure 5. IP3 Performance vs LO Drive Power

5.2 TX band interferer rejection

TX Band Interferer Rejection was tested by injecting an interfering RF signal and an interfering transmit-band signal which is IF apart from the RF signal in frequency into the RF port and the appropriate LO signal to LO port.

For the SA9500 with an IF=85.4MHz,

Cellular FM and CDMA: RF1 (Interferer) = 886.4MHz, -31dBm
 RF2 (TX) = 801MHz, -40dBm
 LO = 966.4MHz, -3dBm
 Measured P_{IF} at IF 85.4MHz
 $TX\ Rej = -31 - P_{IF} + G_c$

where G_c is the conversion gain of the mixer.

PCS CDMA: RF1 (Interferer) = 1965.4MHz, -21dBm
 RF2 (TX) = 1880MHz, -30dBm
 LO = 1022.7MHz, -3dBm
 Measured P_{IF} at IF of 85.4MHz
 $TX\ Rej = -21 - P_{IF} + G_c$

If the IF is so high that the interfering RF frequency corresponding to the lowest TX frequency is out of the receive band, such as IF=210MHz, the TX interferer will be very small. The typical TX band spurious response rejections of the SA9500/SA9502 at 85.4MHz is 61dB in cellular band and 71dB in PCS band.

5.3 IP2

IP2 rejection for the PCS band mixer was measured by applying two RF signals which are nearly 1/2 IF apart to each other and one of which is one IF apart from the LO, to the RF port and measuring the P_{IF} .

For the SA9500 at 85.4MHz IF,

RF1 = 1938.65MHz, -30dBm
 RF2 = 1981.25+0.06MHz, -30dBm
 LO = 1012.025MHz, -3dBm
 Measure IF
 $IIP2 = P(85.4MHz) - P(85.4MHz - 0.12MHz) - 30\ (dB)$

Application of the SA9500/SA9502 dual-band CDMA/AMPS downconverter

AN2002

The typical IP2 rejection in PCS band at 85.4MHz/111.38MHz IF with and without LO doubler is approximately 58dB. If 210MHz IF is used, the corresponding interfering 1/2 RF with 1/2 IF apart is out of the receive band and there will be considerably higher receive path 1/2IF spurious rejection from the band-pass filters.

5.4 Noise Figure

Noise Figure measurement was performed using an HP 8970B Noise Figure Meter. The set-up for SSB Noise Figure measurement of the Cellular Band is depicted in Figure 6. As for the the PCS band, the BP filter must be changed to 1900MHz.

The noise figure of the SA9500/SA9502 vs LO drive power is presented in Figure 7.

When measuring the conversion gain in CDMA mode, do not forget to add the insertion loss of the transformer.

All measurements given above, and the characterization data in the SA9500/SA9502 Data Sheet, are based on 85.4MHz IF for both cellular FM and CDMA modes. For 210 MHz IF in PCS band, the IP3, conversion gain and noise figure measurement results are essentially the same as those at 85.4 MHz IF

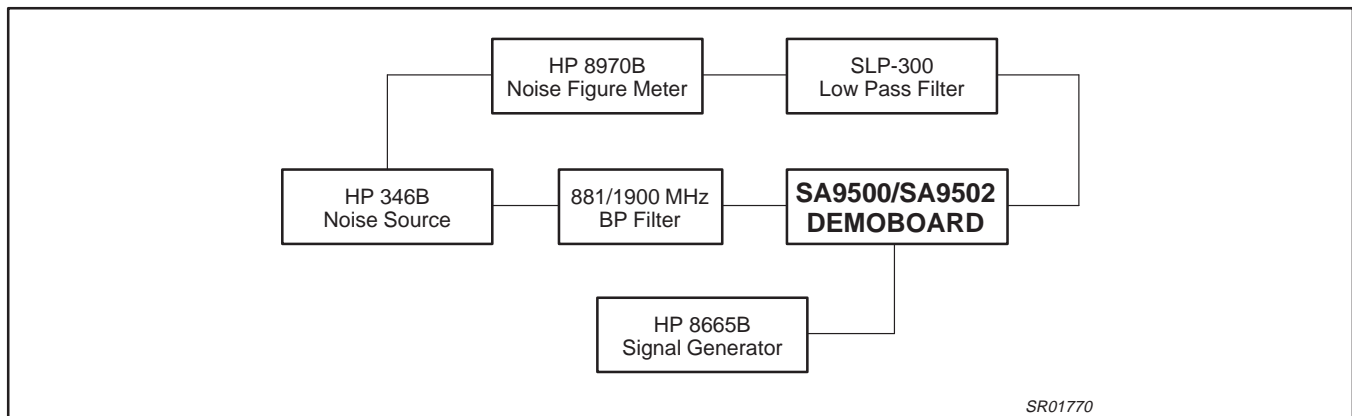


Figure 6. Setup for Noise Figure measurement

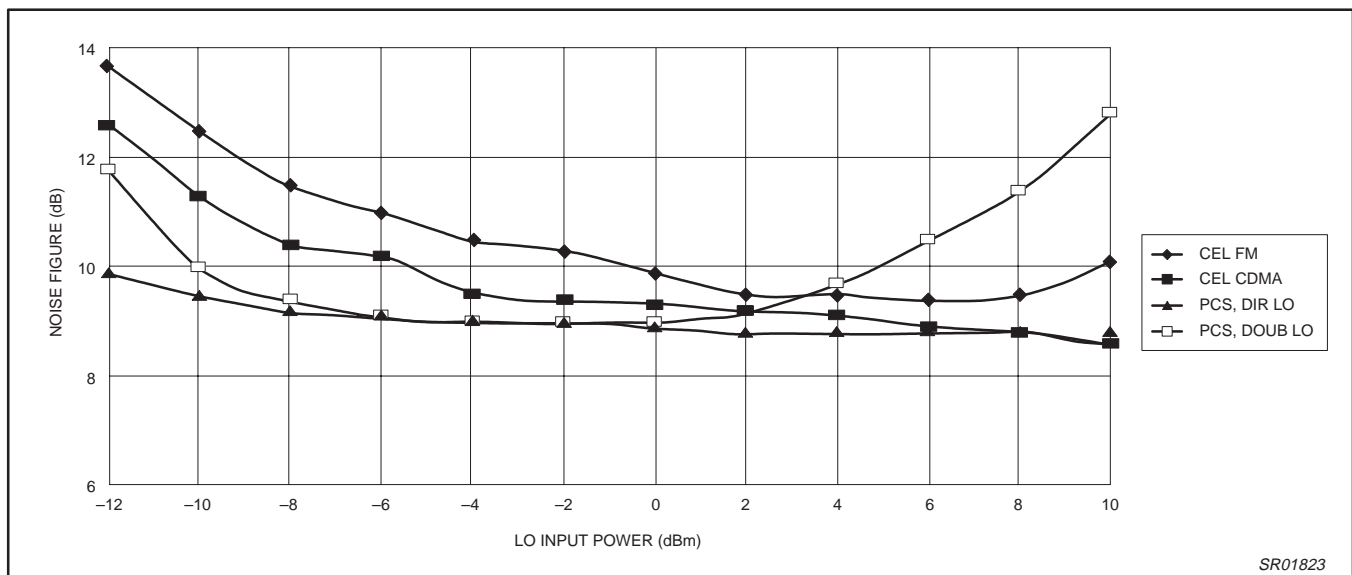


Figure 7. Noise Figure vs LO Drive Power

Application of the SA9500/SA9502 dual-band CDMA/AMPS downconverter

AN2002

6. SOME SUGGESTIONS FOR LNA

For the LNA in front of the SA9500/SA9502, it is recommended to use a Philips Semiconductors wideband discrete bipolar transistor BFG425W, which can provide as much as 16dB gain with noise figure of 1.5dB and IIP3 of approximately +3dBm for both the Cellular and the PCS bands with the appropriate matching networks. The suggested matching networks are shown in Figures 8 and 9, and the typical performance are given in Tables 3 and 5. If higher IIP3 is desired in the Cellular band, then the BFG480W is recommended for 900MHz which can produce as much as +8.5dBm IP3 with a trade-off of current consumption and Noise Figure. The schematic diagram and the performance summary are depicted in Figure 10 and Table 7. For more information on BFG425W or BFG 480W, please refer to the Philips Application Note #KK96-157.

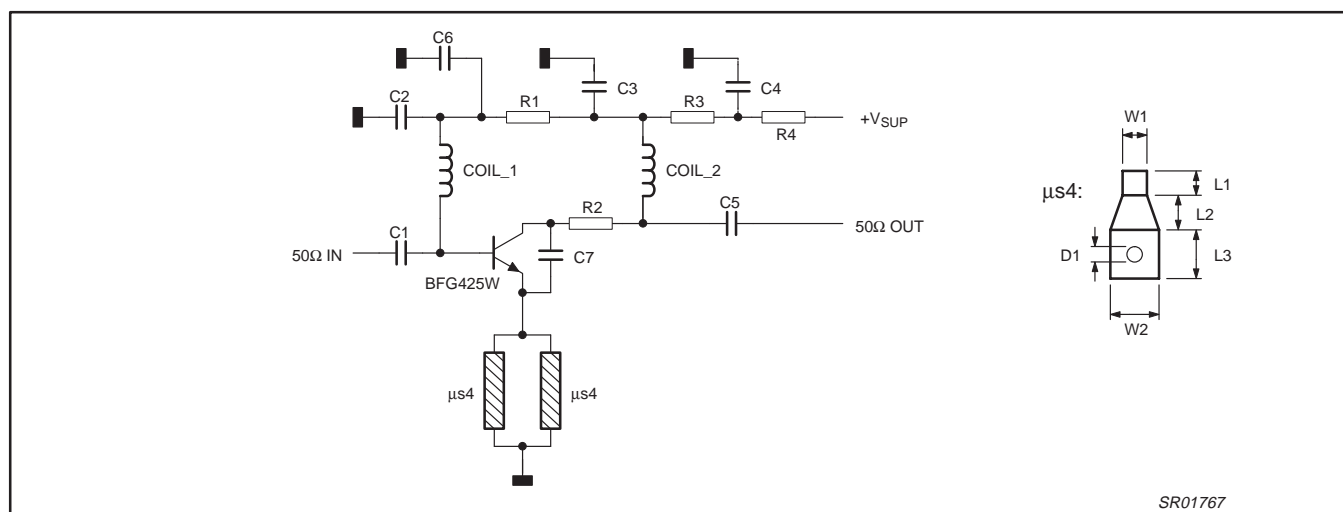


Figure 8. Schematic diagram, 900MHz LNA with BFG425W

Application of the SA9500/SA9502 dual-band CDMA/AMPS downconverter

AN2002

Table 3. Typical performance for 900 MHz LNA with BFG425 W $V_{CE} = 2V$, $I_C = 10mA$, $V_{sup} \approx 3.7V$ $|S_{21}|^2 = 17.3dB$

NF = 1.7dB

VSWR_i = 1:2.5VSWR_o = 1:1.8IP3_{in} = +3dBm ($\Delta f = 200kHz$)**Table 4. Parts list for 900 MHz LNA with BFG425W**Board FR4: $\epsilon_r = 4.6$, $h = 0.5mm$, $t = 35mm$

Coils: 0805CS Coilcraft

COMPONENT	VALUE	PURPOSE, COMMENT
R1 ¹	8.2k Ω	Bias (collector-base)
R2 ¹	10 Ω	better S22 and stability
R3 ¹	2 Ω	RF blocking
R4 ¹	150 Ω	cancelling h_{FE} spread
C1 ¹	8.2pF	input match (input to base)
C2 ¹	27pF	900 MHz short (L1 to ground)
C3 ¹	27pF	900 MHz short (L2 to ground)
C4 ²	100nF	RF decoupling collector bias
C5 ¹	22pF	Output match
C6 ²	100nF	To improve IP3
C7 ¹	3.3pF	Output match, stability
Coil_1	22nH	Input match (base-bias)
Coil_2	12nH	Output match (collector-bias)
$\mu s4$		μ -stripline Emitter-inductance

NOTES:

1. 0603 Philips

2. 0805 Philips

Table 5. Typical performance for 2 GHz LNA with BFG425W

I_C (mA)	$ S_{21} ^2$ (dB)	IP3 (dBm)	NF (dB)
$V_{CE} \approx 2.5V$	2GHz	input	2GHz
2	14.4	-2.3	1.5
3	15.9	-0.4	1.7
5	16.3	1.8	1.8
6	16.6	2.6	1.9
8	16.9	5.6	2.1
10	17.1	6.7	2.3

Application of the SA9500/SA9502 dual-band CDMA/AMPS downconverter

AN2002

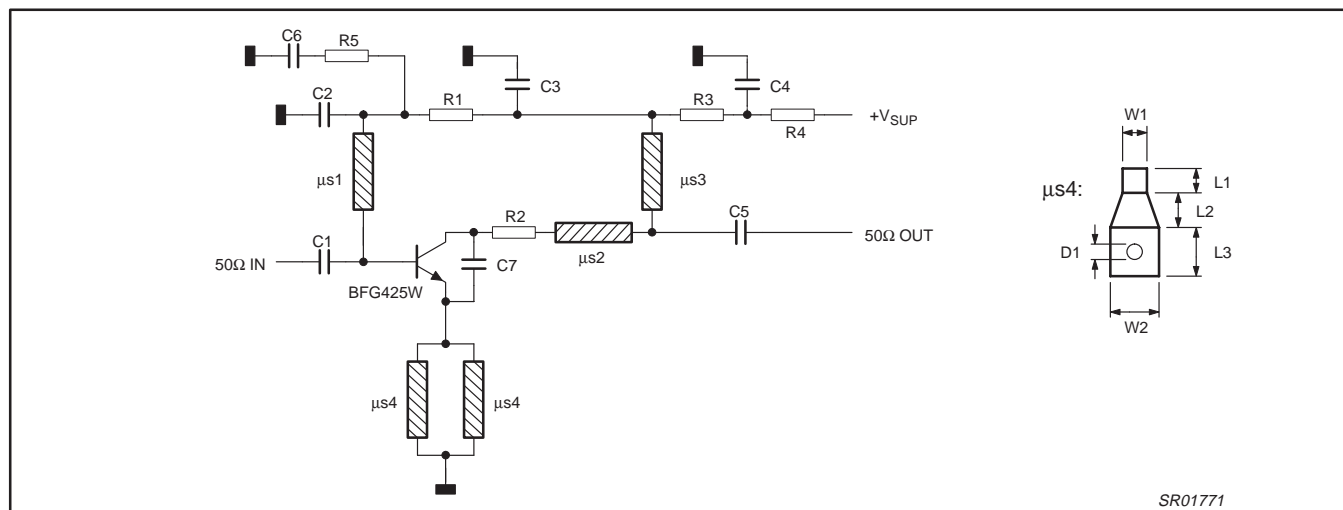


Figure 9. Schematic diagram, 2GHz LNA with BFG425W

Table 6. Parts list for 2 GHz LNA with BFG425W

Board FR4: $\epsilon_r = 4.6$, $h = 0.5\text{mm}$, $t = 35\text{mm}$

COMPONENT	VALUE	PURPOSE, COMMENT
R1 ¹	15k Ω	Bias
R2 ¹	0 Ω	Omitted
R3 ¹	22 Ω	RF blocking
R4 ¹	82 Ω	cancelling h_{FE} spread
R5 ²	100 Ω	To improve IP3 performance
C1 ¹	4.7pF	input match
C2 ¹	5.6pF	2GHz short
C3 ¹	5.6pF	2GHz short
C4 ²	1.0nF	RF-short
C5 ¹	2.7pF	Output match
C6 ²	100nH	To improve IP3 performance
$\mu s1$	8.9mm \times 0.25mm	μ -stripline Z0~95 Ω
$\mu s2$	3.9mm \times 0.25mm	μ -stripline Z0~95 Ω
$\mu s3$	6.6mm \times 0.25mm	μ -stripline Z0~95 Ω
$\mu s4$		μ -stripline + via

NOTES:

- 0603 Philips
- 0805 Philips

Application of the SA9500/SA9502 dual-band
CDMA/AMPS downconverter

AN2002

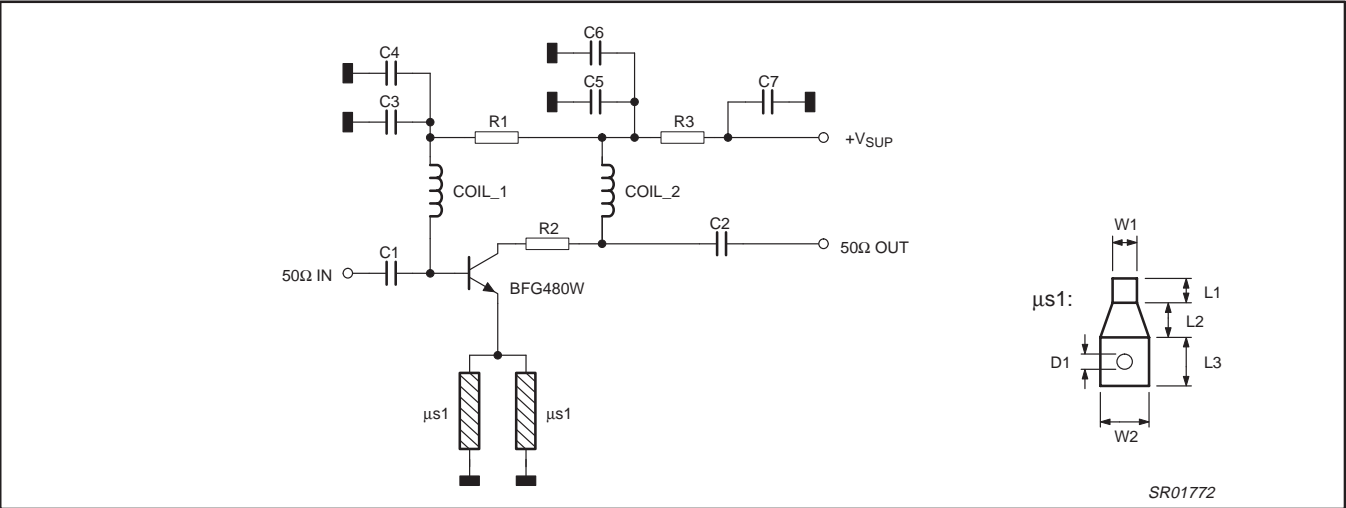


Figure 10. Schematic diagram for 900MHz LNA with BFG480W

Table 7. Performance measurements for 900 MHz LNA with BFG480W

frequency 880 MHz	Measurements
Supply	3.6V; 11.8mA
S ₂₁ ²	12.7dB
VSWR _i	1.35
VSWR _o	1.95
Noise Figure	1.9 dB
IIP3	+8.5 dBm

Table 8. Parts list for 900 MHz LNA with BFG480W

COMPONENT	VALUE	PURPOSE, COMMENT
R1	8.2kΩ	Bias (collector base)
R2	10Ω	Better RF-stability (K-factor > 1)
R3	56Ω	Bias, series with collector, cancelling h _{FE} -spread
C1	27pF	Input match (input to base)
C2	27pF	Output match (collector to output)
C3, C5	27pF	900MHz short (Coil_x to ground)
C4, C6	100nF	Improving IP3 (by decoupling LF IP3 products)
C7	1nF	RF decoupling collector bias
Coil_1	15nH	Input match

Application of the SA9500/SA9502 dual-band CDMA/AMPS downconverter

AN2002

Table 9. Parts list for SA9500 application board

Qty.	Ref. #	Value	Part Number	Manufacturer	Description
Capacitors					
2	C17, C19	1.5pF	0603CG159C9BB0	PHILIPS	Cer Cap 0603 NPO $\pm 0.25\text{pF}$
1	C12	2.2pF	0603CG229C9BB0	PHILIPS	Cer Cap 0603 NPO $\pm 0.25\text{pF}$
1	C10	3.3pF	0603CG339C9BB0	PHILIPS	Cer Cap 0603 NPO $\pm 0.25\text{pF}$
1	C2	6.8pF	0603CG689C9BB0	PHILIPS	Cer Cap 0603 NPO $\pm 0.25\text{pF}$
5	C1, C7, C8, C20, C21	8.2pF	0603CG829C9BB0	PHILIPS	Cer Cap 0603 NPO $\pm 0.5\text{pF}$
2	C4, C5	12pF	0603CG120J9BB0	PHILIPS	Cer Cap 0603 NPO 5%
1	C13	22pF	0603CG220J9BB0	PHILIPS	Cer Cap 0603 NPO 5%
2	C18, C22	33pF	0603CG330J9BB0	PHILIPS	Cer Cap 0603 NPO 5%
2	C6, C11	100pF	0603CG101J9BB0	PHILIPS	Cer Cap 0603 NPO 5%
1	C16	1nF	0603CG102J9BB0	PHILIPS	Cer Cap 0603 NPO 5%
1	C3	10nF	06032R103J9BB0	PHILIPS	Cer Cap 0603 X7R 10%
2	C9, C15	100nF	06032E104J9BB0	PHILIPS	Cer Cap 0603 Z5U 20%
1	C14	10uF			Antalum SMD cap 10 Volts
Resistors					
2	R7, R8	0	2322 702 96001	PHILIPS	Chip Res 1/16W 0603 $\pm 5\%$
2	R5, R6	10 Ω	2322 702 60109	PHILIPS	Chip Res 1/16W 0603 $\pm 5\%$
1	R4	51 Ω	2322 702 60519	PHILIPS	Chip Res 1/16W 0603 $\pm 5\%$
2	R2, R3	680 Ω	2322 702 60681	PHILIPS	Chip Res 1/16W 0603 $\pm 5\%$
1	R1	1.2k Ω	2322 702 60122	PHILIPS	Chip Res 1/16W 0603 $\pm 5\%$
Inductors					
1	L6	3.9nH	LL1608 F3N9K	Toko	Chip inductor 0603 10%
2	L7, L9	4.7nH	LL1608 F4N7K	Toko	Chip inductor 0603 10%
1	L3	8.2nH	LL1608 F8N2K	Toko	Chip inductor 0603 10%
2	L4, L5	180nH	1008HS-181TKBC	Coilcraft	Chip inductor 1008 10%
1	L2	390nH	1008HS-391TKBC	Coilcraft	Chip inductor 1008 10%
1	L1	470nH	1008HS-471TKBC	Coilcraft	Chip inductor 1008 10%
1	L10	TC8-1		Toko	8 to 1 transformer
Integrated Circuits					
1	U1	SA9500			
Connectors					
7	J4, J5, J6, J9, J10, J11	SMA		Johnson	SMA SMD side mount
1	J12	2 PIN			2 pin header, 100 mil spacing
4	J2, J3, J7, J8	3 PIN			3 pin header, 100 mil spacing

Application of the SA9500/SA9502 dual-band
CDMA/AMPS downconverter

AN2002

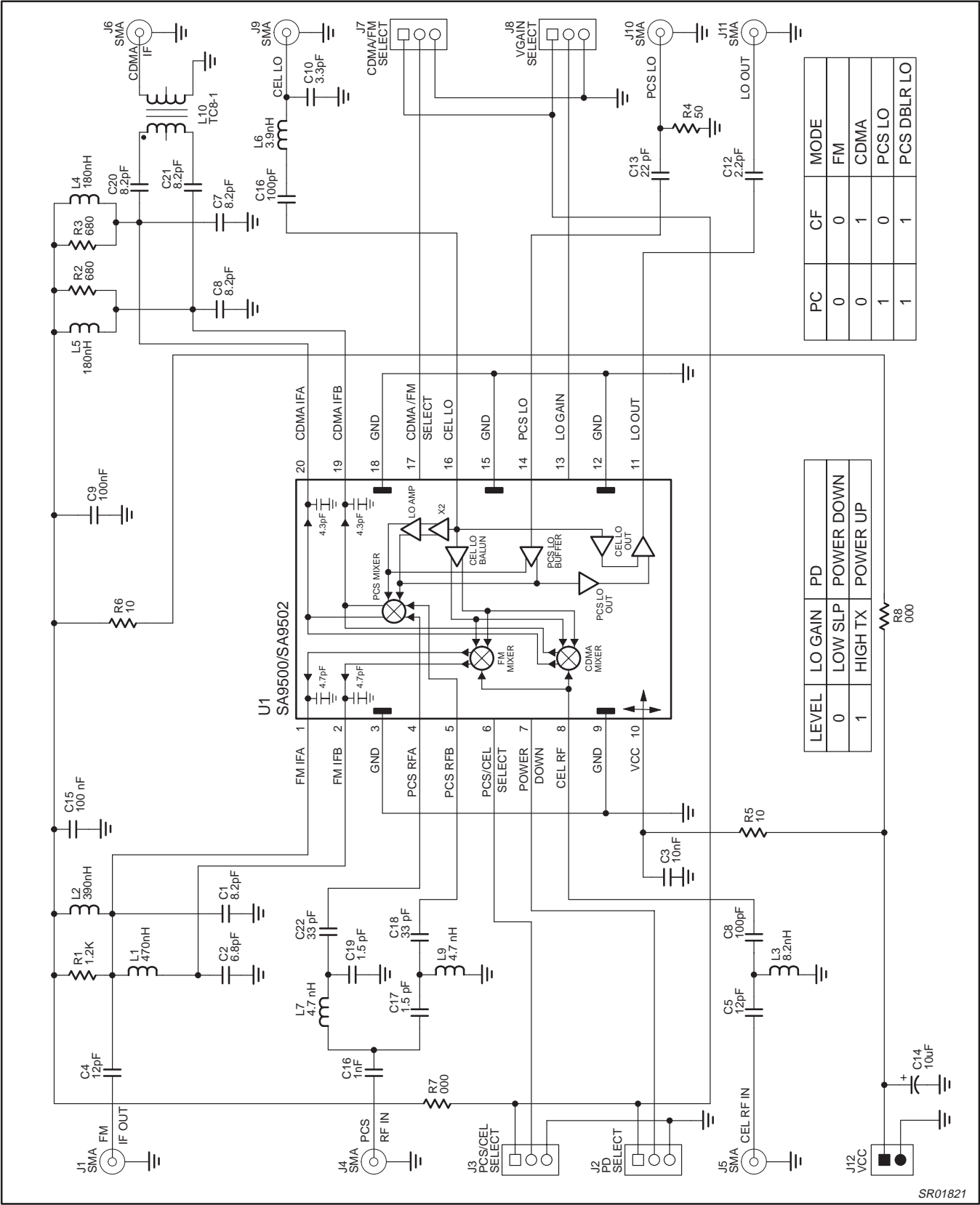


Figure 11. Schematic diagram of SA9500/SA9502 application board

Application of the SA9500/SA9502 dual-band CDMA/AMPS downconverter

AN2002

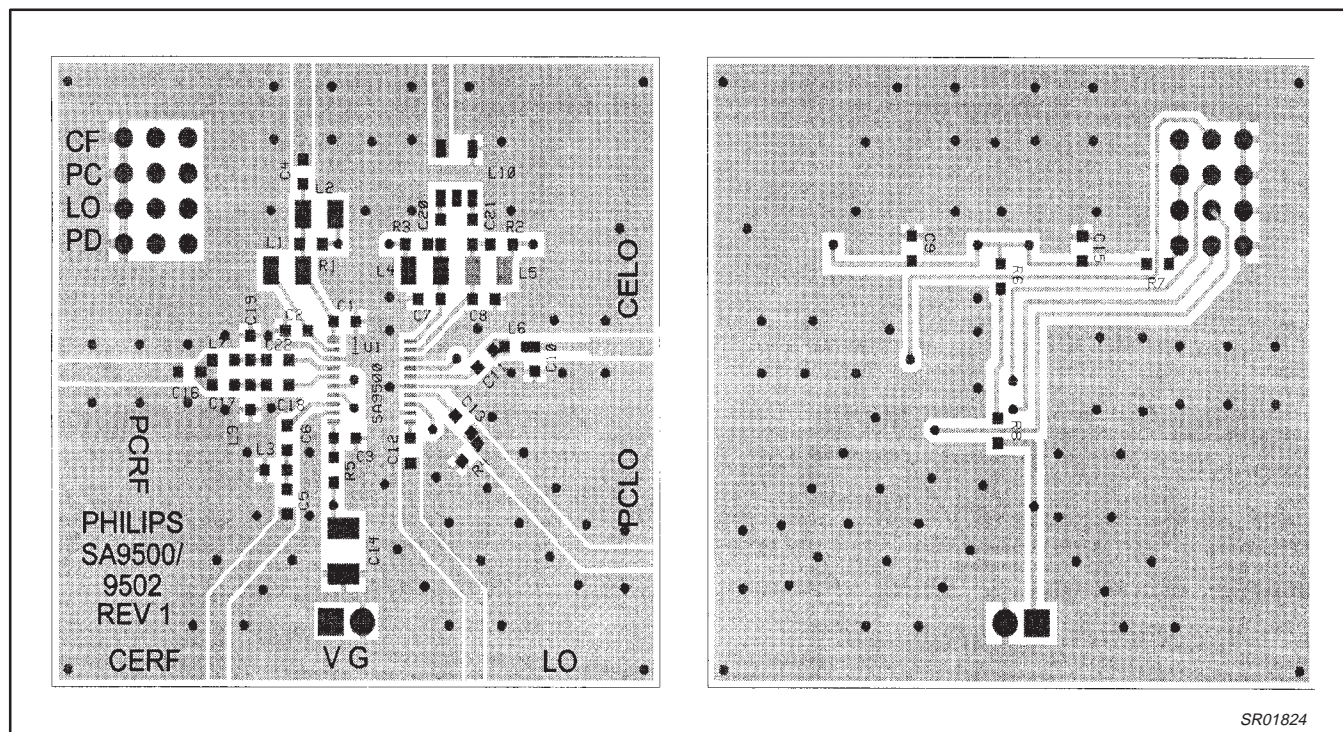


Figure 12. Layout of SA9500/SA9502 application board

7. CONCLUSION

This application note presents a review of the matching circuits for the SA9500/SA9502 and the important measurements. The SA9500/SA9502 combined with the Philips discrete LNA can provide a complete receive front-end solution for a dual-band, triple-mode (CDMA/AMPS) wireless phone. It is capable of high linearity and low noise figure performance to meet the IS-95/98 standards with low current consumption. The wide operating V_{CC} range can be compatible with most phone designs. Using the SA9500/SA9502 also has an advantage of low cost and simplified design.

8. ACKNOWLEDGEMENT

I'd like to cordially thank Jarek Lucek of Philips Semiconductors' Discrete Division for the information provided on the LNA, and also thank Mike Wong and Dai Sieh for their kind help in this project.

9. FREQUENTLY ASKED QUESTIONS AND ANSWERS

Q: Why can't I repeat the single-side band noise figure measurements?

A: The band-pass filter used in the single-side band noise figure measurement is quite important to the results. Different band-pass filters may cause different phase shift so that the input impedance to the board is off the optimum noise figure point and hence the noise figure reading will be varied. We tried three different manufacturers BP SAW filters for the measurement. The measurement variation was as high as 1.0dB. A MuRata BP SAW filter was used for the SA9500/SA9502 characterization.

Application of the SA9500/SA9502 dual-band CDMA/AMPS downconverter

AN2002

Q: How can I match to the high input impedance SAW filters using the current combiner instead of 50Ω?

A: There are very detail descriptions on this topic in Philips Semiconductors Application AN1777. First, normalize the network analyzer to the impedance of interest, then set inductor L2 in Figure 3 to be a large inductance value. Choose “ball park” values for the initial component values based on the simple resonance calculation. Then adjust $C_{1,2}$ and R_1 to obtain the required match.

Q: If I am going to use the differential SAW filters for the IF output instead of single-ended SAW, What kind of match scheme should I use?

A: You can use LC networks to match the two differential output sides separately, each of which should match to half of the input impedance of the SAW filter you are going to use. For example, if the differential input impedance of the SAW filter is 1kΩ, you can select suitable LC networks matching IFA and IFB to 500 Ω respectively.

Application of the SA9500/SA9502 dual-band CDMA/AMPS downconverter

AN2002

NOTES

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AN2002

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 02-99

Document order number:

9397 750 05501

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