AN1682

Using the MC33157 Electronic Ballast Controller

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1 — BASIC HALF BRIDGE ELECTRONIC BALLAST

Most of the European low pressure fluorescent lamps are powered from the mains, using filaments to preheat the tube. Since this type of lamp has a negative going characteristic, as described in Figure 1.1, one must provide a system to control the start up sequence and the steady state current.

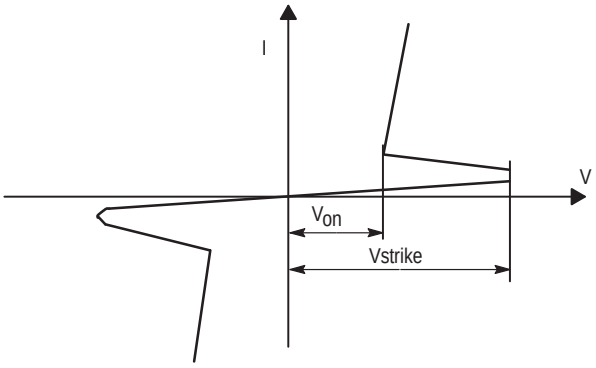


Figure 1.1 Typical Low Pressure Fluorescent Lamp Characteristic

The simple, low cost circuit, is built with a large inductance wired in series with the tube, as depicted in Figure 1.2, the neon bulb being used to strike the lamp. Nowadays, these type of circuits are no longer used and more efficient systems are designed to improve the global performances.

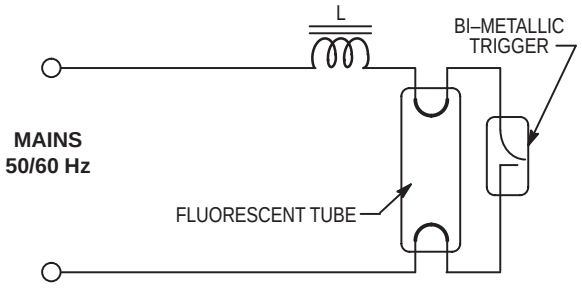


Figure 1.2 Typical Low Cost Fluorescent Circuit

Generally speaking, the electronic ballast must fulfill three major functions:

a – Preheat the filaments
b – Strike the tube
c – Keep the steady state current constant

Of course, all of these characteristics are depending upon the type of lamp, essentially the length of the tube, the glass diameter, the gas pressure and mixture. Several electronic circuits can be designed to implement the functions defined here above, but the most commonly used one, in Europe, is built around a half bridge series resonant network as described in Figure 1.3.

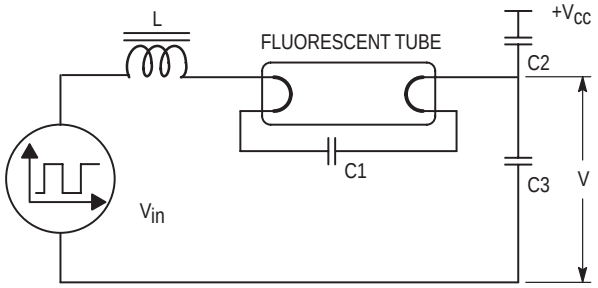


Figure 1.3 Basic Half Bridge Electronic Ballast Series Resonant Circuit

Capacitors C2 and C3 are computed to handle the current flowing into the lamp under both start up and steady state conditions, making sure that voltage V = Vcc/2. When the lamp is OFF, the series resonant network is built with inductor L and capacitors C1/C2/C3. The resonant frequency is given by equation [1.1]:

$$f_o = \frac{1}{2 * \sqrt{(L * [\frac{C1 * (C2 + C3)}{C1 + C2 + C3}])}} \quad [1.1]$$

However, since C2 = C3 and C1<< (C2 + C3), capacitors C2 and C3 can be, generally, neglected and equation 1.1 can be simplified as :

$$f_o = \frac{1}{2 * \sqrt{(L * C1)}} \quad [1.2]$$

In order to predict the behavior of the circuit, it is recommended to plot the impedance of the resonant network as a function of the frequency. Figure 1.4 gives an example highlighting the influence of the L/R ratio in this application.

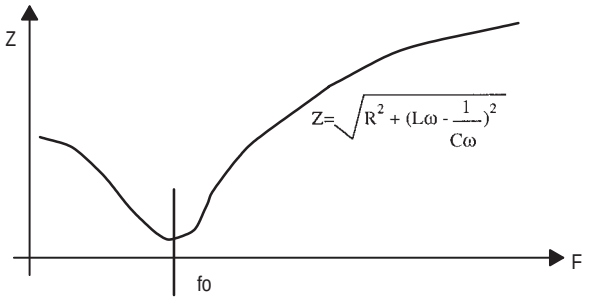


Figure 1.4 Typical Resonant Circuit Function

At this point, the value of the inductance L can't be freely defined, but is calculated based on several parameters:

– mains voltage : sets up the Vcc value
– fluorescent tube : defines Vstrike and Von
– frequency : defines the steady state operating frequency F

On the other hand, the inductance limits the current flowing into the tube and must be designed according to the expected level of power:

$$Ptube = Von * Itube \quad [1.3]$$

Since the input pulse is supposed to have a 50% duty cycle, the value of inductor L can be calculated by using the Lentz's law:

$$L = \frac{V_L * dt}{dI} \quad [1.4]$$

To turn ON the tube, the system must generate the strike voltage across the end electrodes. The quality factor parameter — Q — is used to fulfill this function, the minimum value of Q depending on the fluorescent lamp and Vcc characteristics:

$$Q > (2 * Vstrike)/Vcc \quad [1.5]$$

and

$$Q = \frac{L\omega}{R} \quad [1.6]$$

Generally speaking, the value of resistor R comes, mainly, from the filaments of the fluorescent tube, but the total value of R might be adjusted to increase the damping of the Z impedance.

Once all the parameters are identified, the resonant network can be calculated, using the operating frequency as a reference. Although such a circuit can operate in a first pass application, three main points make it not straightforward usable in the industry:

a – The Power Factor is well below the 0.94 specified by the EEC regulations.
b – The output power varies as the line voltage varies within the 185–265 V European span normalization.
c – The circuit must fulfill the THD class A specification.

Consequently, one must implement the extra circuits, as depicted in Figure 1.5, to make the electronic ballast module suitable for EEC applications.

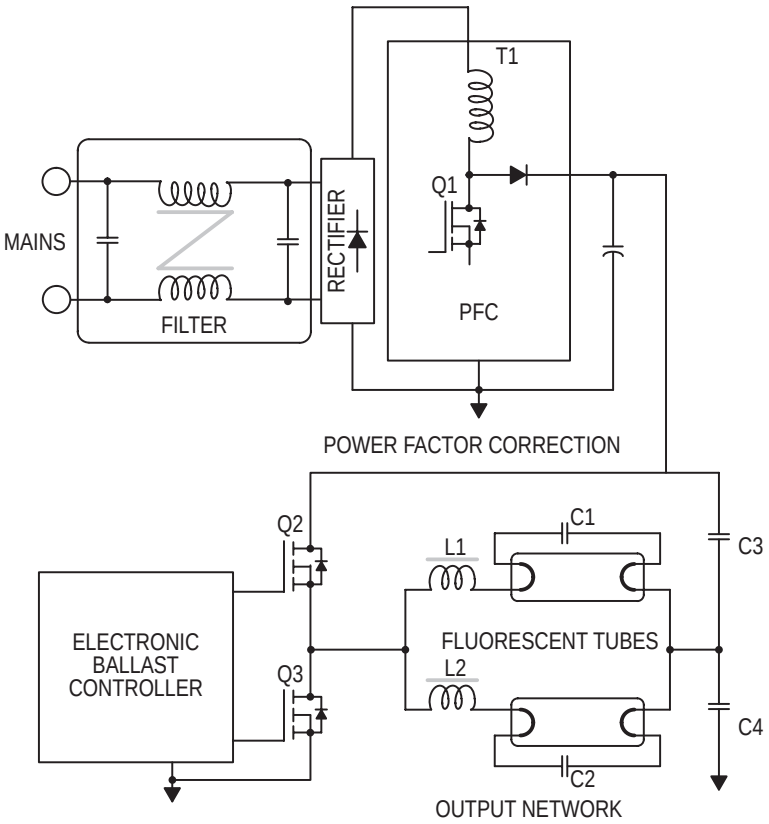


Figure 1.5 Basic EEC Industrial Electronic Ballast

Since this Application Note is focused on the electronic ballast controller, the reader will get the technical informations related to the Power Factor circuit in the Motorola Linear data book (see MC33262 data sheet).

2 — MC33157 DESCRIPTION

The purpose of the MC33157 is to implement all the basic functions needed to operate an electronic ballast. This integrated circuit comes in a 16 pin SOIC package and can run 10A/500 V power MOSFET operated up to 250 kHz. A simplified internal circuit, depicted in Figure 2.1, together with the data sheet, are useful to understand the MC33157.

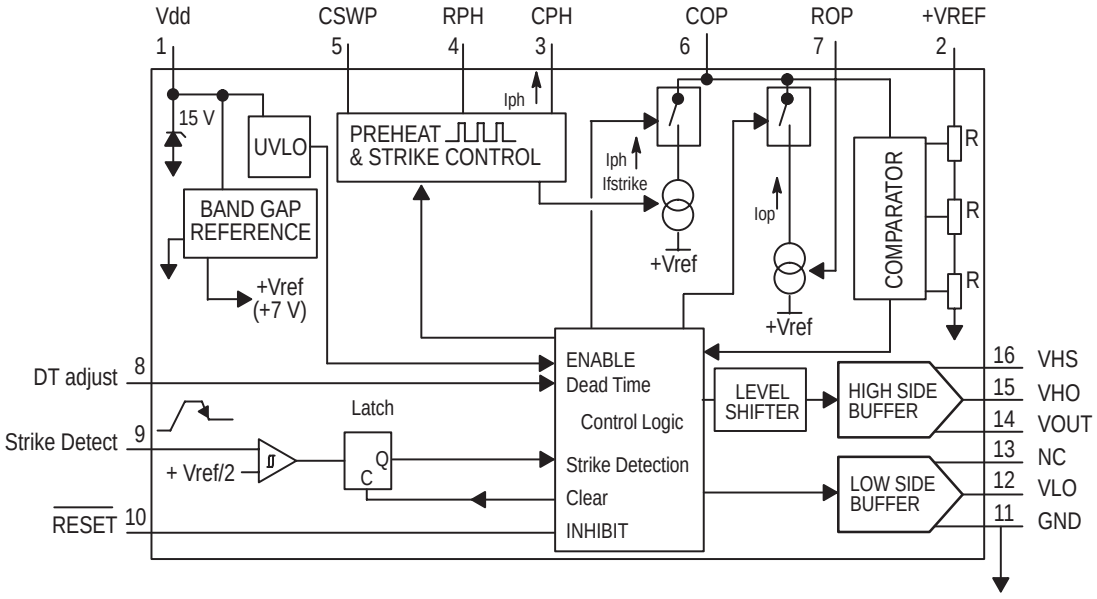


Figure 2.1 Simplified MC33157 Internal Circuit

2.1 Reference Voltage

The 7 V reference voltage — Vref — is generated by the internal band gap, yielding a ± 2.0% tolerance over the –20°C to + 85° C ambient temperature range. This voltage reference is 100% trimmed at probe level during the manufacturing. All the MC33157 built in circuits are derived from this reference. On top of that, the reference voltage is made available pin 2 to supply the external components and can source up to 25 mA. Practically, it is recommended to bypass Vref to ground with a 220 nF ceramic capacitor.

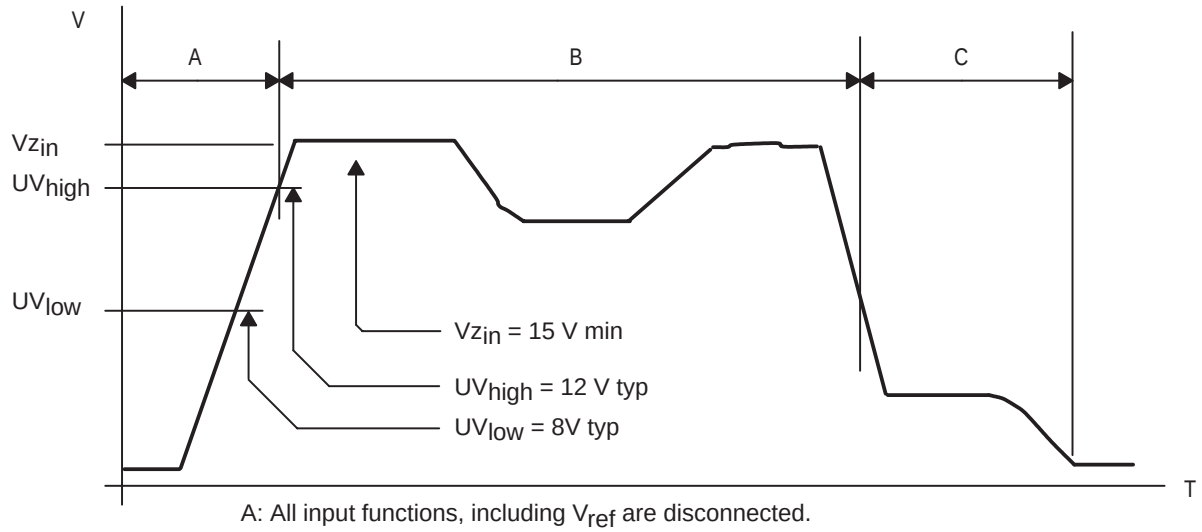
The High side and Low side boosters are capable to handle, respectively, 250 mA and 300 mA into the gate of external power MOSFET, with a 15 V gate to source voltage capability. The totem pole topology yields current transient as fast as 30 ns when loaded by a 8 A rated power MOSFET, with capacitance gate peak current above 1 A. The MC33157 data sheet gives the details of these two circuits.

2.2 Power Supply

The power supply, connected pin 1, provides the energy to the controller and the integrated circuit monitors the low and high voltage input value. To operate the controller, the input supply voltage must rise above 12 V, the dV/dt being not important as long as it is slower than 1 V/ns.

According to the timing described Figure 2.2, the system is in OFF state until Vdd > 12 V, and all the internal functions, except the voltage reference, are disconnected. When the input voltage becomes higher than 12 V and stays within the 12 to 8.5 V span, the system operates normally and all the internal functions are active. On the other hand, the built in zener can absorb short voltage spikes, but is not designed to regulate the Vdd supply. It is up to the designer to make sure that the supply voltage never exceeds, continuously, the 15 V specified in the data sheet.

As soon as the power supply voltage drops below 8.5 V, the system is stopped and all the internal functions are disconnected. To resume the circuit, one must rise the power supply up to 12 V minimum again as described below.



A: All input functions, including V_{ref} are disconnected.
B: All input functions, including V_{ref} are activated and operate normally.
C: All input functions, including V_{ref} are disconnected.

Figure 2.2 Supply Voltage Operation

The internal zener circuit clamps the input voltage to 15 V, but protection must be taken, externally to the MC33157, to limit the clamp current at 15 mA under worst case condition. This is particularly important when wide excursions of the power supply are expected in the application. In this case, it is recommended to connect an extra 15 V external zener across Vdd to ground to avoid any inrush current into the internal clamp.

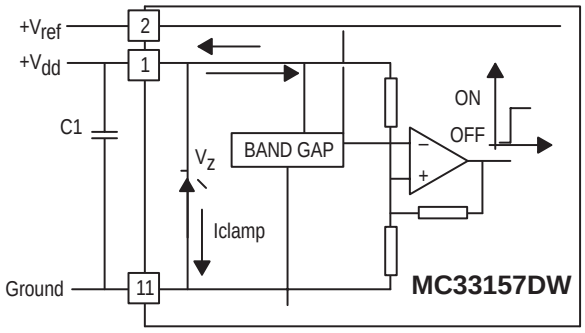


Figure 2.3 Basic Voltage Supply Detection

Most of the time, the +Vdd voltage comes from a limited power source and capacitor C1 is mandatory to supply the energy to the output high and low side boosters. Usually, a 22 µF/25 V electrolytic is large enough to fulfill this function.

2.3 Filaments Preheating

During the start up sequence of a fluorescent lamp, one must provide the power to preheat the filaments, improving the ignition of the tube and increasing its expected life time. Beside the output boosters, the controller takes care of the timing expected by the designer. This function is achieved by a current source charging an external capacitor as depicted in Figure 2.4.

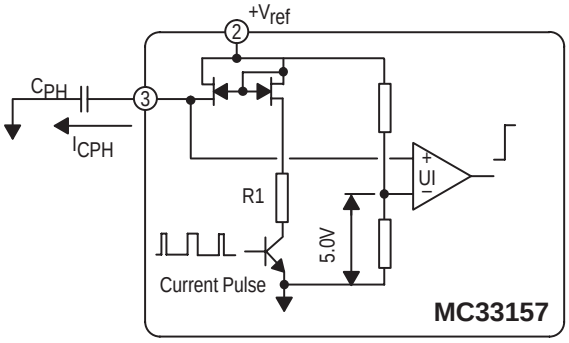


Figure 2.4 Preheating Capacitor Current Source Control

Resistor R1, internally connected from +Vref to ground, setup the current through the built–in current mirror which, in turn, charges capacitor C_{PH}. When the voltage across this capacitor reaches 5 V, the comparator U1 flips to a high state and the system jumps to the sweep mode. Figure 2.5 gives the main states of the MC33157 during the start up sequence.

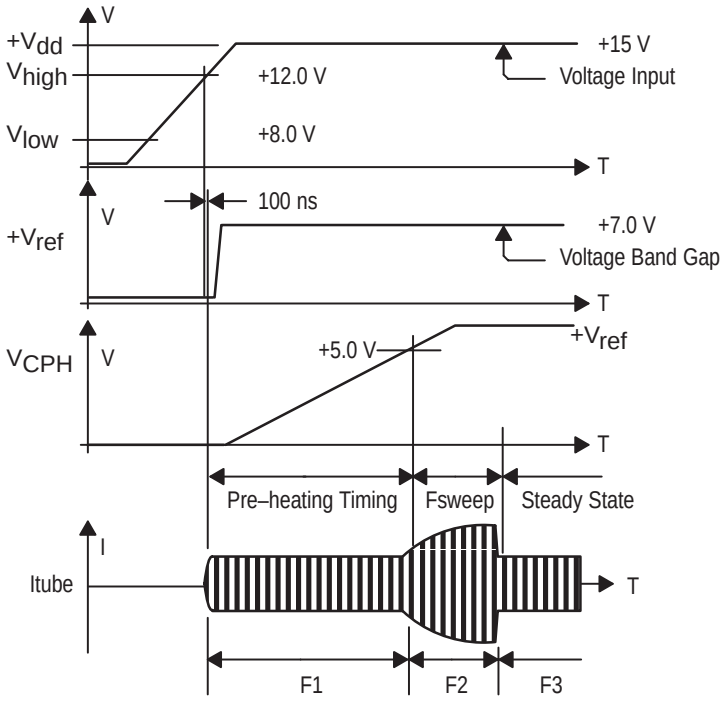


Figure 2.5 Electronic Ballast Filament Preheat Timing

To achieve a two second long timing with a 0.47 µF polyester capacitor, a specific current source topology has being used in the chip. The concept is to charge the capacitor with a pulsed current, as described in Figure 2.6, to decrease the dV/dt across the C_{PH} capacitor. Assuming the leakage current of the capacitor is lower than 10 nA, the system gives the expected timing with a low cost standard non electrolytic capacitor.

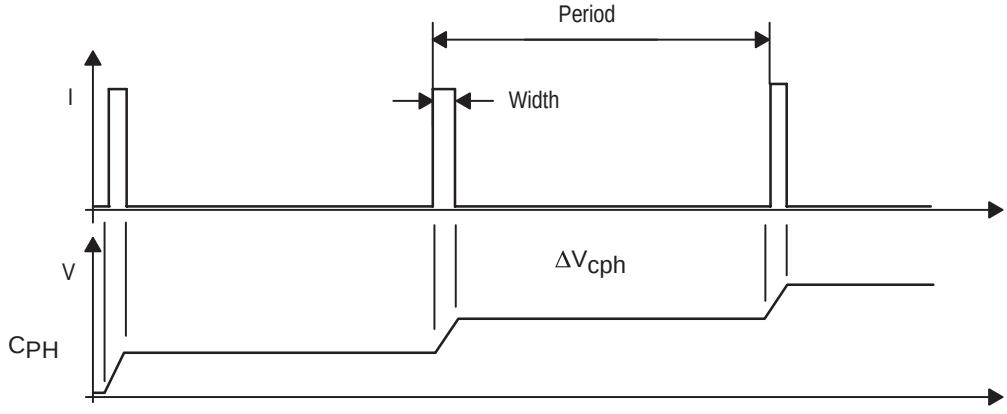


Figure 2.6 Basic Pulsed C_{PH} Timing

Since both the period and the width of this current are derived from the main clock of the integrated circuit, the duty cycle is constant:

DC timing = Width/Period

DC timing = 1/16

On the other hand, the internal comparator flips when V_{CPH} rises above 5.0 V, with a 2.0 V hysteresis, and the circuit can be calculated straightforward. Since the current is constant, then:

$$Tph = \frac{C_{PH} * V_{CPH}}{I_{CPH} * DC} \quad [2.1]$$

By rearranging the constant values, equation [2.2] can be used once the time T_{ph} is defined by the designer, assuming I_{CPH} = 16 µA peak:

$$C_{PH} = \frac{Tph * 10^{-6}}{5} \quad [2.2]$$

Of course, a low leakage capacitor together with high quality pcb clad, is preferably selected to implement C_{PH} when long timing are expected.

2.4 Oscillator Operation

The oscillator is used as a main clock to control both the internal logic and the output boosters. The frequency is derived from the integration of the external capacitor C_{OP} by either current R_{PH} and R_{SWP} or I_{OP} as described in Figure 2.7.

The electronic switches SW1 and SW2 are used to select the current source as defined in Table 2.1 below:

Table 2.1 Current Source Selection

	Q1	SW1	SW2	C_{OP}
Preheat	ON	ON	OFF	i1 = i2 + i3
Frequency shift	OFF	ON	OFF	$i1 = i2 + i4*e^{-t/T}$
Steady state	OFF	OFF	ON	i1 = Iop

These switches are controlled by the MC33157 internal logic and cannot be accessed by the external circuit. However, it is possible to get a specific frequency shift, for a given application, by using a different current source to supply pin 4. In this case, cares much be observed to avoid any over–voltage or over–current in any of the integrated circuit inputs.

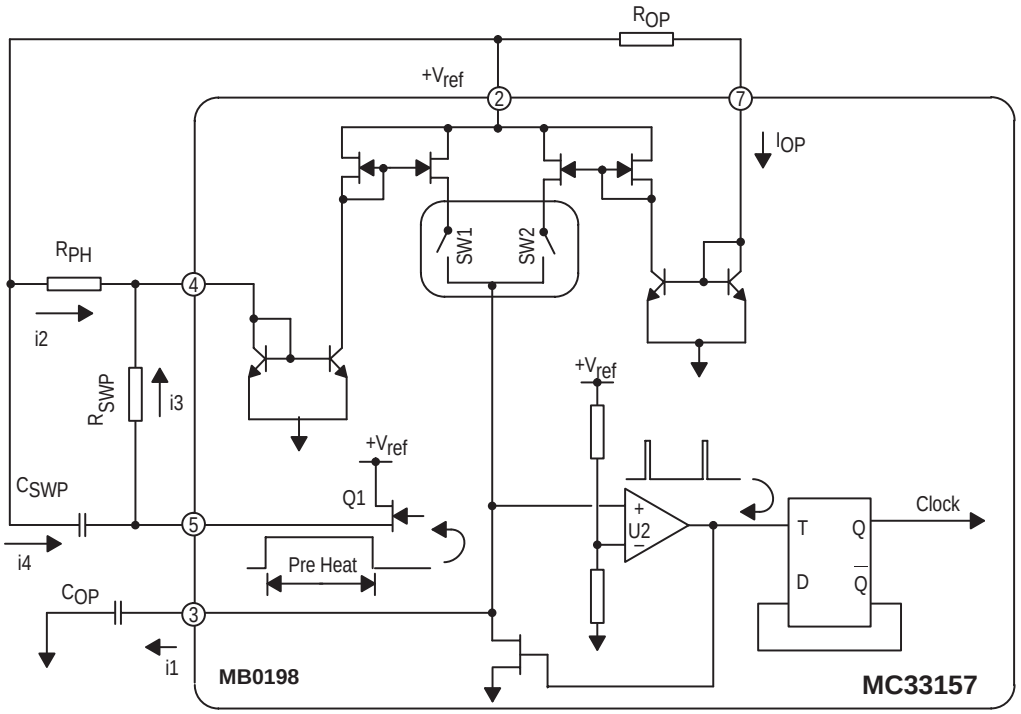


Figure 2.7 Simplified Frequency Operation Circuit

2.5 Strike Operation

As already described above, the comparator U1 flips to a high state and the system jumps to the sweep mode when the voltage at pin 3 reaches 5 V. At this moment, the current i_3 is no longer supplied by Q1, but comes from the integration of capacitor C_{SWP} and the frequency is modulated to generate the strike voltage across the resonant network.

Once the preheating is completed, the controller shifts the frequency from the initial value to the one defined by the designer. This is achieved by the current modulation coming from the C_{SWP} capacitor as depicted in Figures 2.8 and 2.9. Consequently, the end frequency — F2 — is always lower than the start up frequency F1. On the other hand, the frequency modulation moves the operating curve of the L & C network along the resonance, as depicted in Figure 2.8, yielding the high voltage expected to ignite the lamp. In the event of a strike, the high voltage collapses immediately, since the resonant network is damped by the fluorescent tube low impedance, and the controller jumps to the steady state mode, forcing the frequency to the value — F3 — defined by the designer.

If the lamp does not strike, the system repeats four time the frequency sweep mode and comes to a full stop if no strike is detected after the last fourth cycle.

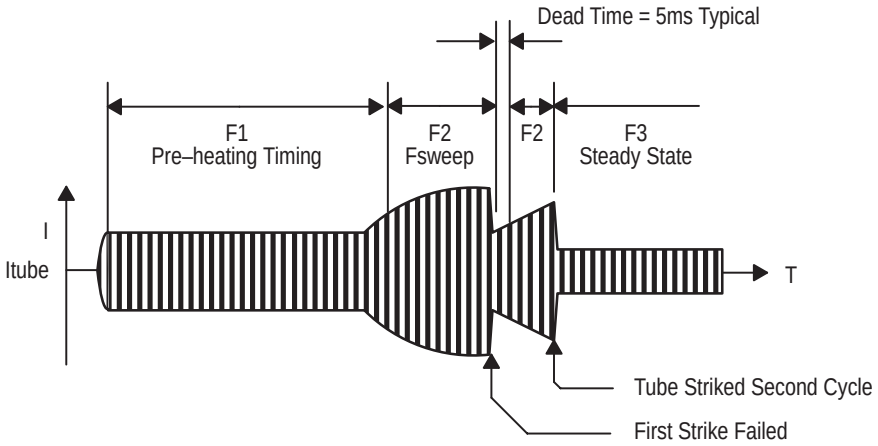


Figure 2.8 Preheat and Strike Cycles Timing

If the lamp does not strike, the system creates a 5 ms dead time between the last frequency sweep and the next one as depicted in Figure 2.8. Such care is mandatory to avoid a false strike detection when the resonant current drops from the peak value to the start up condition. On the other hand, the controller enables the strike detection as soon as the start up sequence begins. In fact, the strike voltage depends upon several parameters (ambient temperature, pressure, end of life lamp, new lamp, ...) and a fluorescent lamp might jump to the normal operation at any time during the preheating sequence.

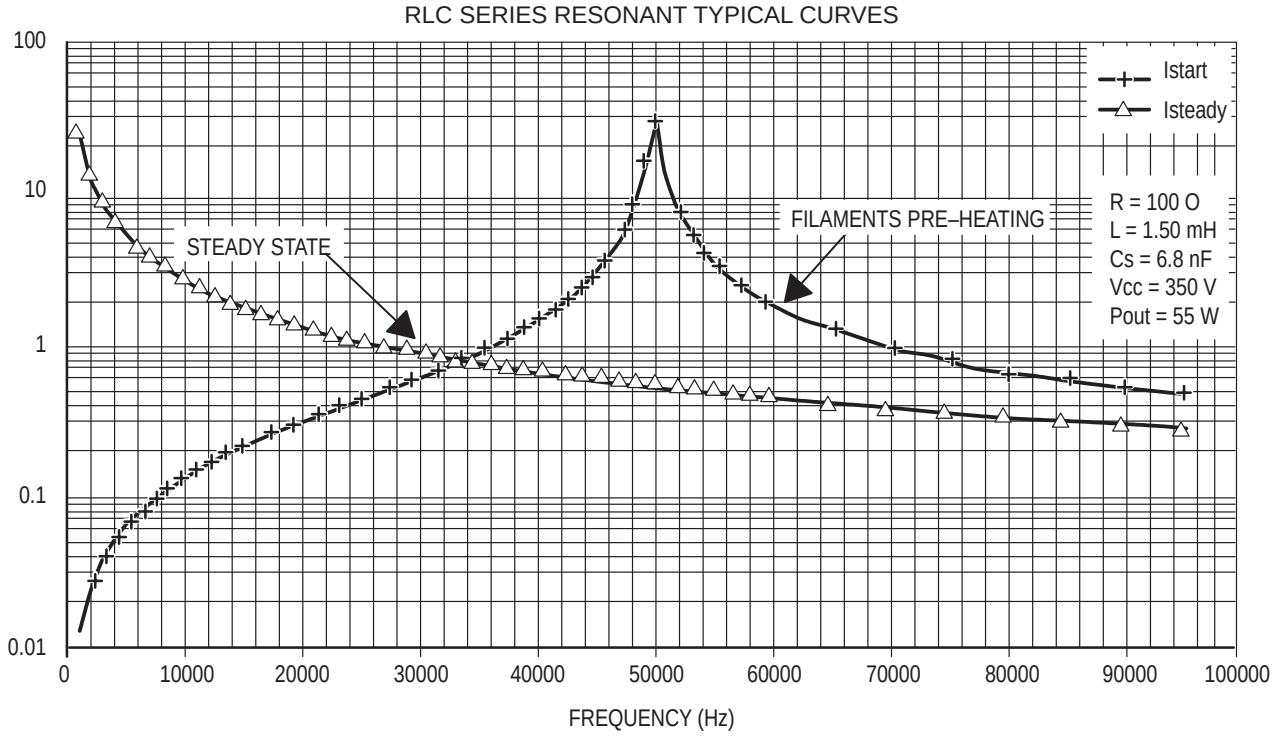
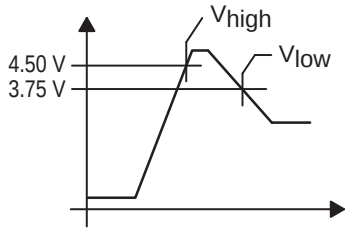


Figure 2.9 Resonant Circuit and Frequency Modulation Behavior

Beside the ignition sequence, the system must be made aware of the status of the lamps. This is implemented by pin 9 which provides an analog input to the signal coming from the external circuit as depicted in Figure 2.10. The critical parameters are the two threshold levels:

Vhigh = 4.50 V: this level preset the internal comparator to a high state

Vlow = 3.75 V: this level confirm the lamp(s) have struck



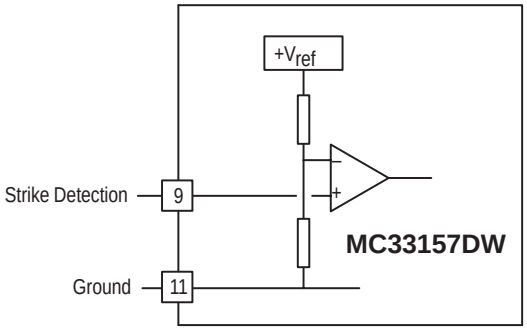


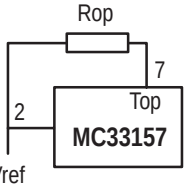
Figure 2.10 Electronic Ballast Typical Strike Voltage Sense and Timing

The internal logic activates the controller according to the signal presents at pin 9, this function being de–asserted as soon as the system operates in steady state. The dV/dt is not important when limited to 5 kV/µs, but cares must be observed to avoid false detection coming from the electrical noise present in this kind of application.

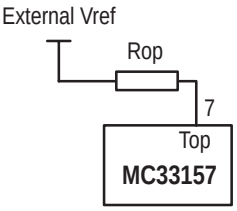
2.6 Steady State Operation

When the start–up sequence ends, the controller forces the system into the steady state mode. The frequency is now the one defined by the designer, using the current into pin 7 for that purpose. In the mean time, the strike detection input is deactivated and the signal present pin 9 is not sensed by the controller. The timing from C_{PH} keeps going but does not generate any logic or analog action within the MC33157 chip, except when a RESET is asserted pin 10.

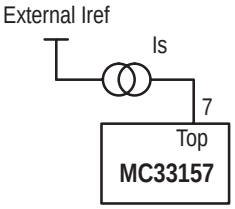
Since the oscillator is built with a current controlled function, the frequency can be easily modulated or controlled by external circuit. Figure 2.11 gives typical applications to drive pin 7.



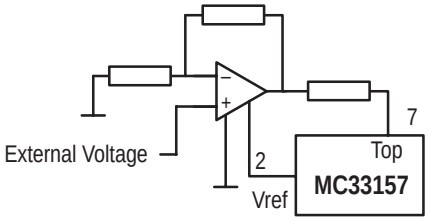
Standard Fop using Built–in Vref



External Voltage Controlled Fop



External Current Controlled Fop



External Control Loop and/or Modulation

Figure 2.11 Electronic Ballast Steady State Typical Controls

The power control applied to the output lamps can be implemented by using a loop built with an external operational amplifier connected to pin 7 as given in Figure 2.11. Similar circuit can be used to dim the light out of the fluorescent lamps.

2.7 Reset Function

A fast reset function is provided pin 10 to control the operation of the MC33157. This pin is level sensitive, non latched, negative logic, with CMOS equivalent input.

When the RESET is activated by pulling pin 10 to a low level, the system stops, forcing the two output power MOSFET to the OFF state (both gates are connected to their respective source). When the logic level at pin 10 is released, the RESET is deactivated and the system runs a strike sequence as depicted in Figure 2.12, the preheating of the filament being not performed. All the frequencies are the one defined by the external resistors (R_{PH} and R_{OP}) and capacitor C_{OP}. On the other hand, since C_{PH} is grounded when the RESET is activated, the system generates five ignition sequence, the first frequency sweep period being two time longer than the four following one. One must point out that it is necessary to internally ground capacitor C_{PH} to make sure the system will restart from a fully defined state when the RESET will be cleared.

A built in 20 uA source makes sure the RESET is at high level when pin 10 is left open. This function being not latched, it can be combined with external OR gates to get complex behavior. The evaluation board uses this pin as an input to force the re–lamping as depicted in Figure 3.1.

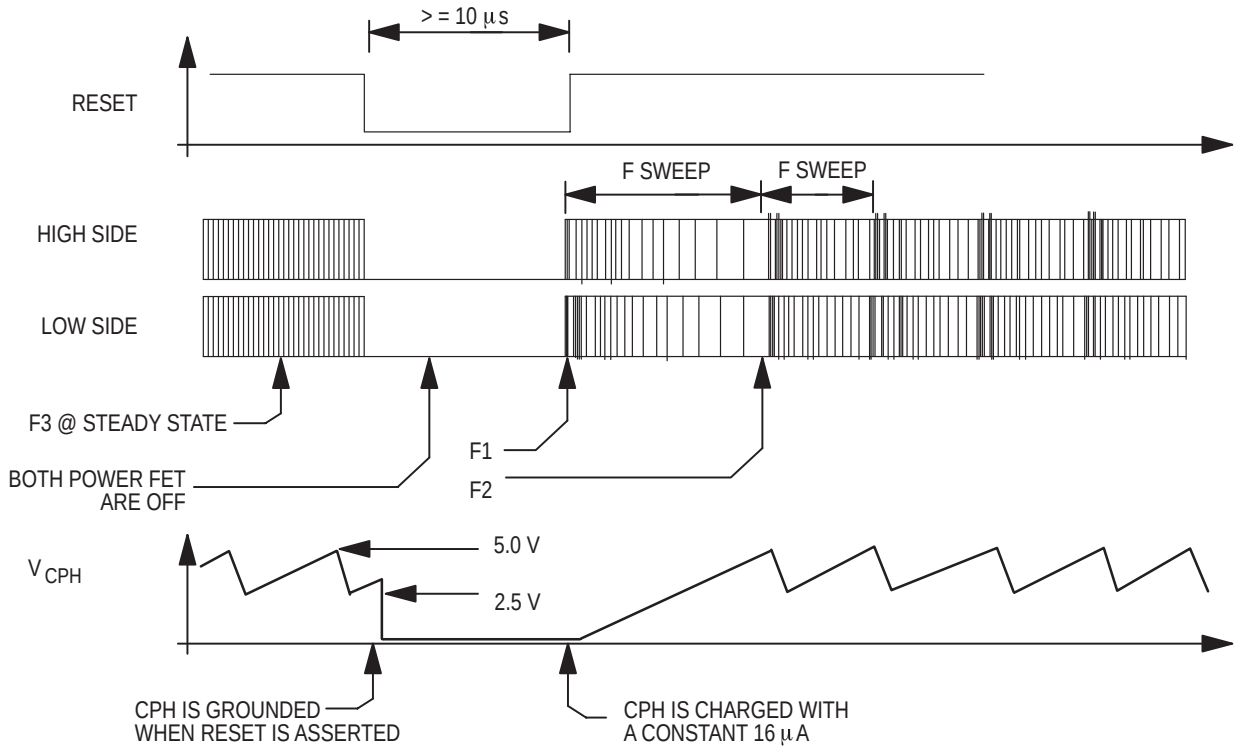


Figure 2.12 RESET Operation

The RESET logic trigger voltages have being designed to provide a strong hysterisis, avoiding uncontrolled function coming from the noise. This function uses a negative logic:

Input pin 10	RESET
0 V ––> 1.8 V	Activated :true
> 1.8 ––> 7 V	Deactivated :false

It is recommended to minimize the pick up noise coming from the environment entering the RESET pin. The pcb lay out must be design in this respect and a 100nF/ceramic capacitor must be used to bypass pin 10 to ground.

The most critical point is probably the ground path: there must be a single return point to the power ground and no output power current shall flow in the same track. The evaluation board has been designed to avoid any uncontrolled power loop in the MC33157DW ground.

3 — ELECTRONIC BALLAST CONTROLLER APPLICATION

Note: the application described here below is designed to operate a dual 55 W tube module, powered from the 230 V nominal line voltage. All the circuits described here after are referenced to the schematic diagram given in Figure 3.1.

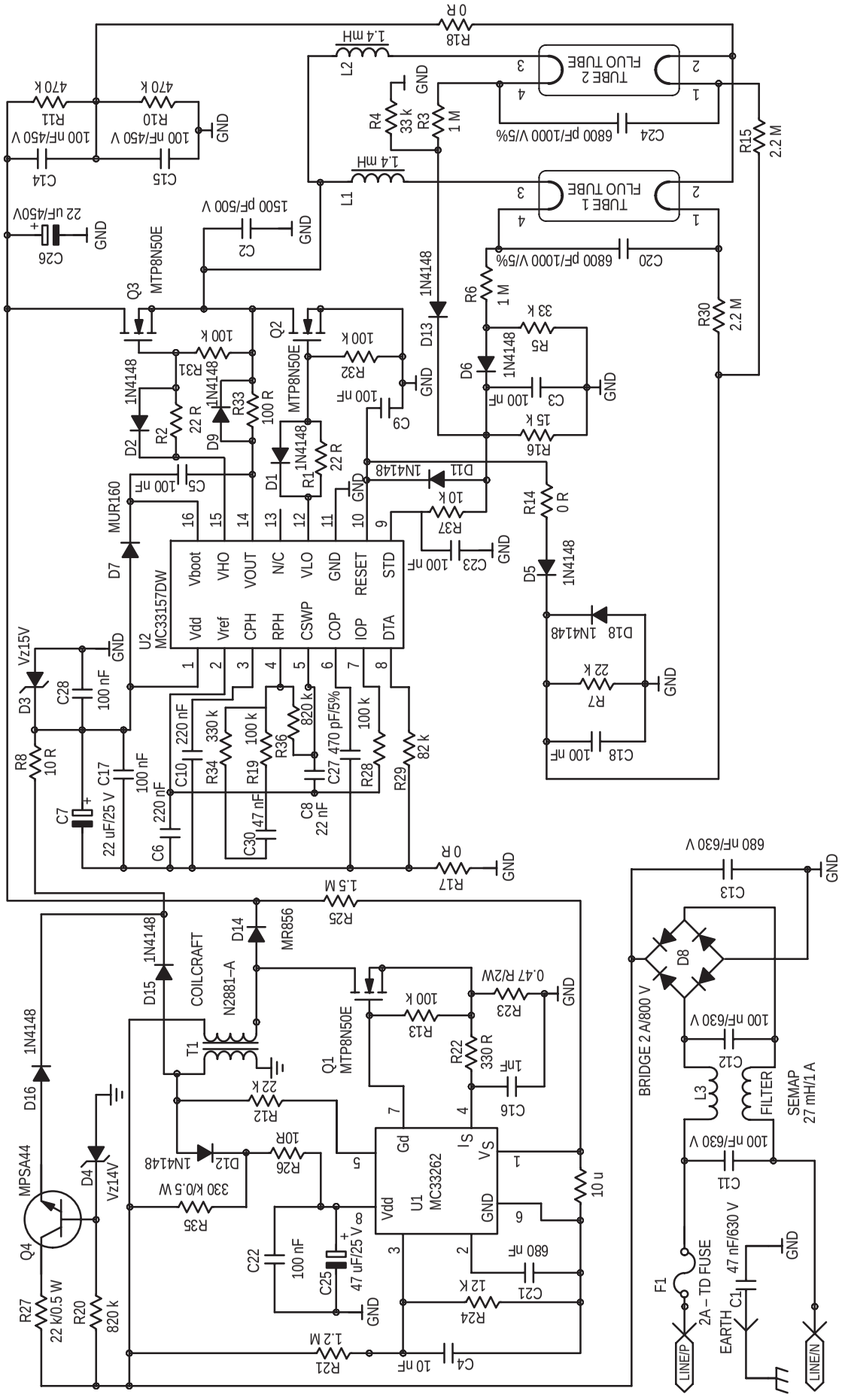


Figure 3.1 Typical Industrial Application Electronic Ballast

OSCILLATOR CAPACITOR C_{OP}

All the frequencies used by the controller (preheating, strike and steady state) come from the integration of accurately controlled current into the external capacitor C_{OP}. The Turn On time is adjusted externally, either by a single set of resistors connected to +Vref, or by means of a current coming from an auxiliary circuit. Figure 3.2 gives a simplified schematic of the C_{OP} circuit.

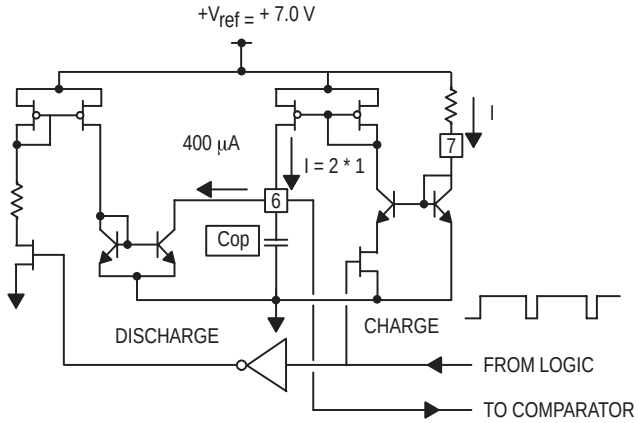


Figure 3.2 Simplified C_{OP} Operating Circuit

The Turn Off time is defined by the internal constant 400 µA used to discharge capacitor C_{OP}. This current is not externally adjustable.

The Delay Time never exceeds 50 ns and cannot be adjusted externally.

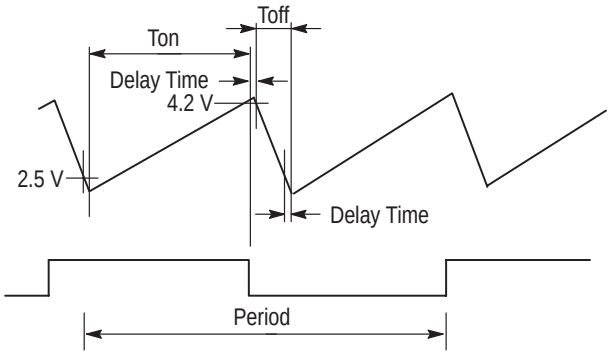


Figure 3.3 Basic Oscillator Capacitor Timing

At any time, the frequency can be externally programmed to cope with specific needs, but the source current flowing into the circuit pins 4, 5 or 7 or must not exceed 2 mA per pin. On the other hand, the designer must take into account the stray capacitance presents pin 7 when calculating the oscillator. Typically, pin 6 parasitic internal capacitance is 15 pF.

Timing Calculations

$$ton = \frac{C_{OP} * dV}{2 * I} \quad [3.1]$$

Since the threshold voltages are constant and accurately given by the internal circuit, let Vthlow = 2.8 V and Vth_{high} = 4.2 V. Equation [3.1] can be simplified as:

$$ton = \frac{C_{OP} * (Vth_{high} - Vth_{low})}{2 * I} \quad [3.2]$$

$$ton = \frac{C_{OP} * 1.4}{2 * I} \quad [3.3]$$

On the other hand, since capacitor C_{OP} is discharged by a constant 400 µA current, we can derive the toff timing:

$$toff = \frac{C_{OP} * dV}{400 * 10^{-6}} \quad [3.4]$$

The threshold voltage being the same than the ton timing, then:

$$toff = \frac{C_{OP} * 1.4}{400 * 10^{-6}} \quad [3.5]$$

and:

$$toff = C_{OP} * 3500 \quad [3.6]$$

PRACTICAL NUMERICAL EXAMPLE

Let's define C_{OP} = 470 pF and F = 60 kHz in steady state. The period time shall be:

$$T = \frac{1}{2 * F} = \frac{1}{2 * 60 * 10^3} = 8.33\ \mu s$$

The turn off time needed to discharge C_{OP} is:

$$toff = C_{OP} * 3500 = 470 * 10^{-12} * 3500 = 1.64\ \mu s$$

The turn on time of the same capacitor is derived from the expected operating frequency and the turn off time calculated here above:

$$ton = T - toff = 8.33 - 1.64 = 6.69\ \mu s$$

The external programmed current — I — is then calculated by rearranging equation [3.3]:

$$I = \frac{C_{OP} * dV}{2 * ton} = \frac{470 * 10^{-12} * 1.4}{2 * 6.69 * 10^{-6}} = 49.17\ \mu A$$

The value of resistor R_{OP}, which is connected between pin 7 and +Vref, with Vbe and Vgs equal to the internal thresholds, is:

$$R_{OP} = \frac{Vref - Vbe - Vgs}{I} \quad [3.7]$$

$$R_{OP} = \frac{7 - 0.6 - 2}{49.17 * 10^{-6}} = 89.485\ k\Omega$$

Let us select the normalized 91 kΩ value from a E24/ ± 5% series. The calculation of the frequency adjust resistor value can be derived from the graph given in Figure 3.4 below.

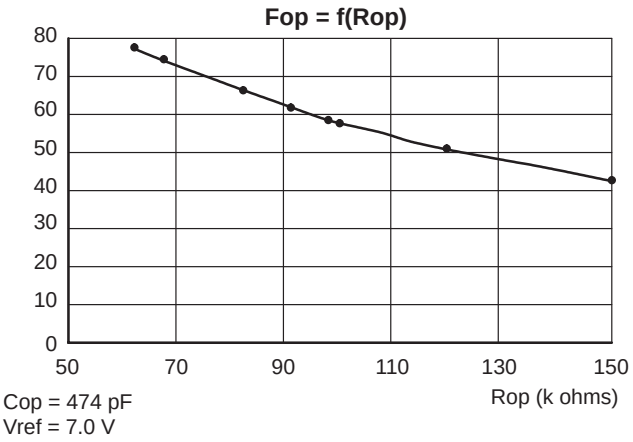


Figure 3.4 Frequency Operation Fop = f(Rop) for a given 470 pF Oscillator Capacitor

PREHEATING TIMING AND FREQUENCY ADJUST

The preheating time comes by integration of an accurate pulsed current into the external capacitor C_{PH}. When the voltage across capacitor C_{PH} crosses the built–in +5 V reference, the preheating time is completed and the system jumps to the frequency sweep state. One must point out that if no capacitor are connected from pin 3 to ground, the preheating time is in the micro second range and the system goes immediately to the sweep mode.

Assuming the leakage current around pin 3 is negligible (below 10 nA), then capacitor C_{PH} can be derived as follows:

$$C_{PH} = \frac{Ich * t}{Vph * \delta} \qquad [3.8]$$

The current Ich is internally set up to 16 µA. The ratio — δ — is fixed to 1/16 and Vph represents the constant 5.0 V threshold. For an expected preheating time of 750 ms, then:

$$C_{PH} = \frac{16 * 10 - 6 * 0.75}{5 * 16} = 150 \text{ nF}$$

During the preheating time, capacitor C_{SWEEP} is internally shorted to +Vref by means of a low impedance MOS, thus connecting resistor R_{PH} to +Vref. Consequently, the oscillator capacitor C_{OP} is charged by the sum of currents I1 and I2 as depicted in Figure 3.5.

On the other hand, the internal MOS is turned off when the preheating time is completed, capacitor C_{SWEEP} is now charged by the current flowing from Vref through R_{PH} and the net current going to C_{OP} will reduce until C_{SWEEP} is fully charged. At this point, the frequency is the one defined solely by the net value of current I1, hence the value of resistor R_{ENDSWP}.

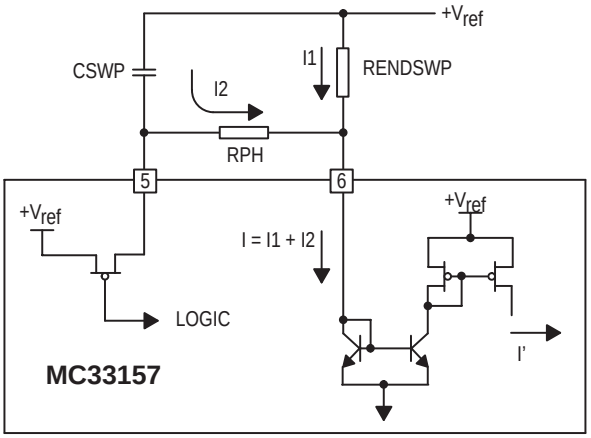


Figure 3.5 Preheating Network

To simplify the analysis of the circuit, let us consider the end of the sweep period, assuming capacitor C_{SWEEP} is fully charged. Of course, the resonant behavior of the RLC series network connected across the supply and the lamp, must be analyzed prior to run the timing and frequency calculations here below. In particular, the designer must accurately define the shape of the resonant curve to make sure the system will operate in a safe area together with a guaranteed strike of the lamp under the worst case conditions.

When capacitor C_{SWEEP} is fully charged, no current flows into resistor R_{PH} and the charge of capacitor C_{OP} comes from current I1 only. Using equations derived before, one can calculate the value of resistor R1 for a given resonant RLC curve. Since we make the frequency F2 identical to the value of F3 in steady state (60 kHz), then:

T = 8.33 µs toff = 1.64 µs ton = 6.69 µs I1 = 49.17 µA

R_{ENDSWP} = 89.485 kΩ—> 91 kΩ normalized

Next, we can calculate the value of resistor R_{PH} needed to set up the frequency during the preheating time. Based on the RLC curve, let F1 = 65 kHz. Using the same method as used before, then:

T = 7.69 µs toff = 1.64 µs ton = 6.05 µs I = 54,38 µA

Since resistor R_{ENDSWP} supplies 49,17 µA, resistor R_{PH} must provide the rest:

$$I2 = I - I1 = 54,38 - 49.17 = 5,21 \text{ µA}$$

Then:

$$R_{PH} = \frac{7 - 0,6 - 2}{5,21 * 10^{-6}} = 844.529 \text{ kΩ} --> 820 \text{ kΩ}$$

normalized

Figure 3.6 gives the typical MOSFET gate voltages and the current flowing in one lamp.

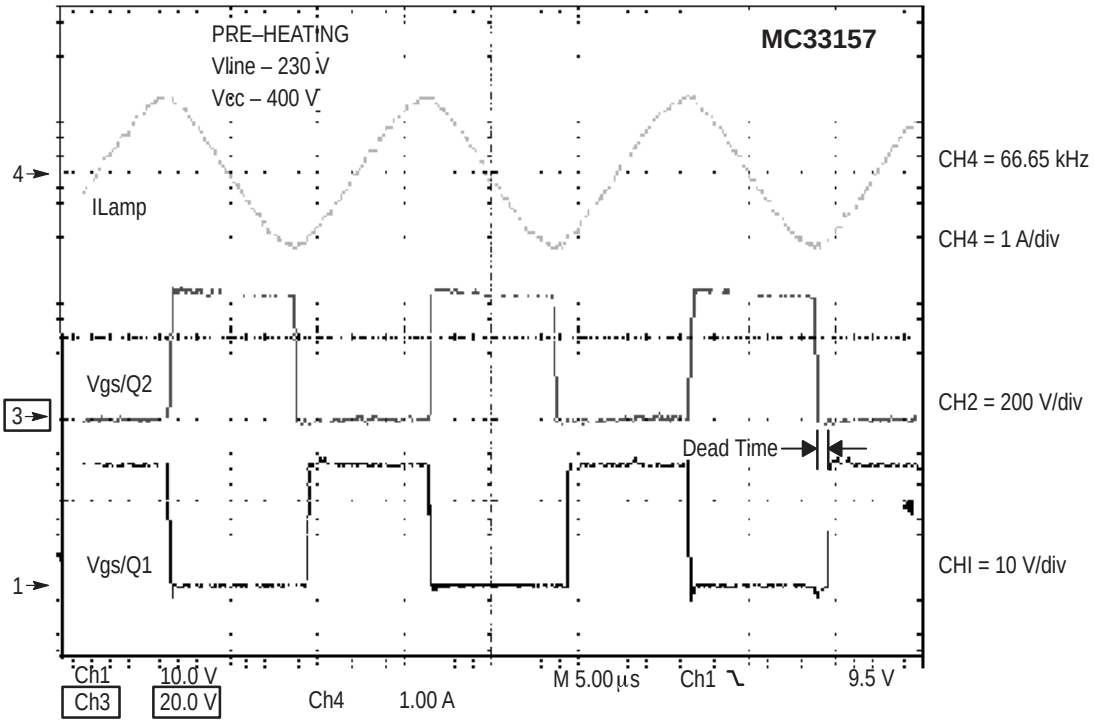


Figure 3.6 Preheat Typical Operation

Although the preheating of the filaments is not very complex, one must avoid large inrush current when the filaments are cold. Such behavior will significantly reduce the expected life time of the lamp by downgrading the electrodes. Thanks to the flexibility of the MC33157, this mechanism is easily overcome by using a current modulation during the first decades of milliseconds of the preheating sequence. As a matter of fact, since the oscillator is controlled by a current, one can modulate the frequency, hence the current flowing into the external load, as depicted in Figure 3.7.

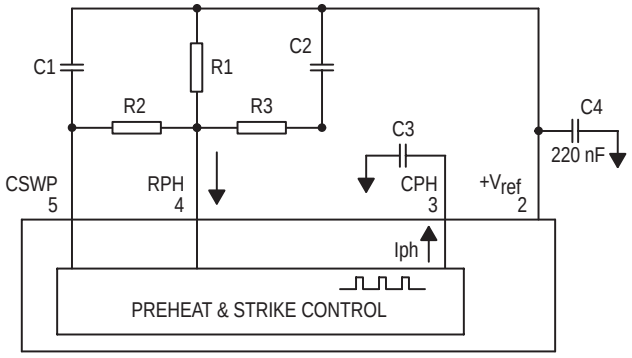


Figure 3.7 Extra Filament Preheating Prevent Cold Inrush Current

The frequency sweep is a function of the resistor R3 connected in series with capacitor C2. When the Vdd supply turns ON, capacitor C2 charges exponentially, yielding a current through R3 into the node at pin 4. Consequently, the preheating frequency smoothly sweep from a high value to the one defined by R1 and R2. The PSPICE equivalent circuit typical behavior is given in Figure 3.8.

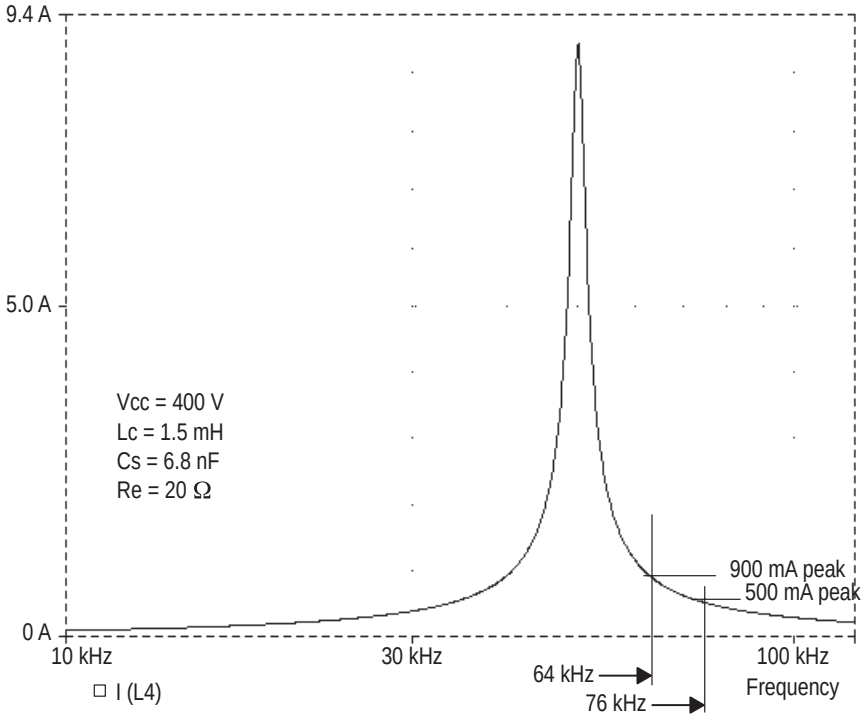


Figure 3.8 Typical Extra Filament Preheating Simulation Function

The frequency sweep is calculated in the next paragraph.

FREQUENCY SWEEP

When the preheating time ends, the system automatically activates the frequency sweep by removing the internal short across capacitor C_{SWP}. Consequently, the current into R decreases as capacitor C_{SWP} charges exponentially. Since the sum of I1 + I2 decreases, the frequency decreases as well, yielding a shift from F1 to F2 as calculated here above.

The sweep timing is generated by forcing a DC current into capacitor C_{PH}, associated with a new set of threshold voltages (2.80 V low, 4.10 V high). Since the internal circuits are built with controlled current and voltages, a 1/8 constant time ratio between preheating and sweep is maintained by the system.

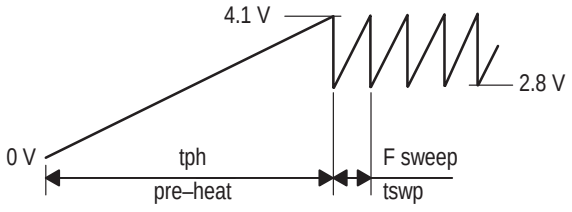


Figure 3.9 Basic Preheating Timing

The controller provides a sweep to reach the strike point located on the curve of the resonant network as defined by the design engineer. Generally speaking, the end frequency F2 shall be activated during the last milliseconds of the frequency sweep. Consequently, current I2 must be zero before the end of this timing. Using the preheating time defined above, the frequency sweep timing will be:

$$tswp = tph/8 = 0.75/8 = 93.7 \text{ ms}$$

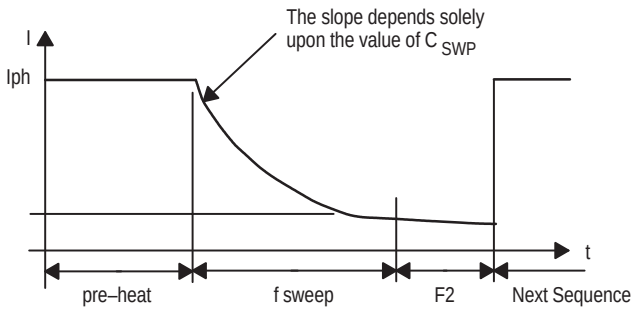
The CSWP time constant comes from resistor R:

$$\theta = CSWP * R, \text{ hence } T = 5 * \theta$$

Assuming we expect a 30 ms operating time under F2 frequency, then:

$$CSWP = \frac{T}{5 * R} = \frac{(93.7 - 30) * 10^{-3}}{5 * 910 * 10^{3}}$$

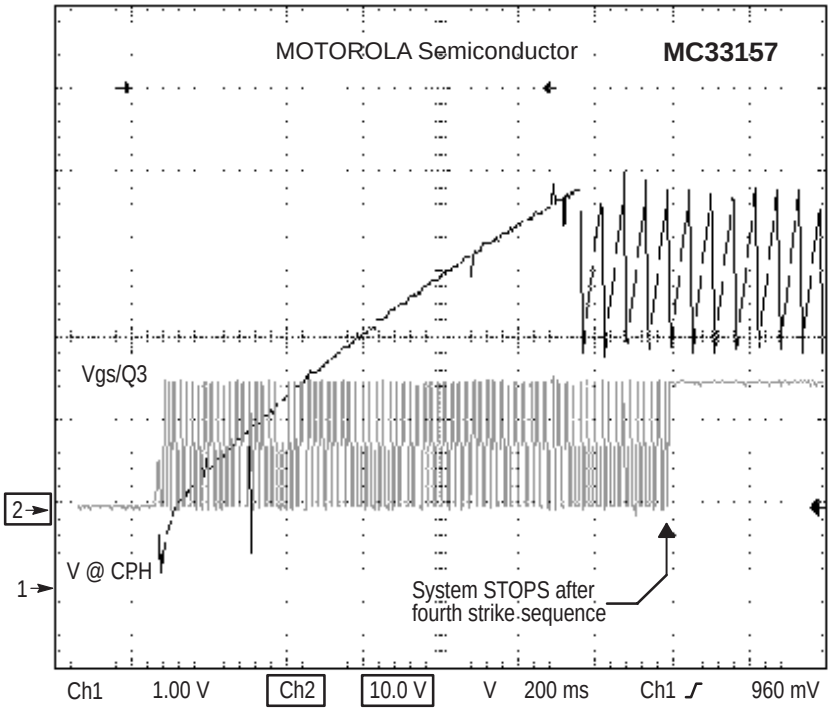
$$= 14 \text{ nF} --> 15 \text{ nF normalized}$$



Note: Curve is not to scale.

Figure 3.10 Basic Frequency Sweep Timing

At this point, all the oscillators are defined and we can calculate the rest of this circuit. Figure 3.11 gives the normal operating waveforms recorded in the evaluation board. In this example, no lamps are connected to the load to highlight the start up sequence under fault condition.



Note: Since the impedance of the probe used to record this waveform is limited to 10 Meg, the slope of the voltage across CPH appears not linear as depicted here above. It is purely linear when no load is connected across capacitor CPH during a normal operation, or when observed with a high impedance buffer.

Figure 3.11 Start–up Sequence with no Strike Lamp Detected

DEAD TIME

The Dead Time depends upon the snubber capacitor, hence the dV/dt of the output voltage. Let the dV/dt = 2kV/µs, yielding a 1500 pF snubber capacitor, to cover the range of operation. The dead time must be longer than the delay coming from the snubber circuit:

$$dt > \frac{Csnub * Vcc}{I} = \frac{1500 * 10^{-12} * 400}{\sqrt{1.8}} = 447.3 \text{ ns}$$

With a 1 µs dead time value, including safety margin, the resistor is derived from the MC33157 set of curves provided in the data sheet, yielding a 82 kΩ normalized value. Figure 3.12 illustrates the dead time used in this example.

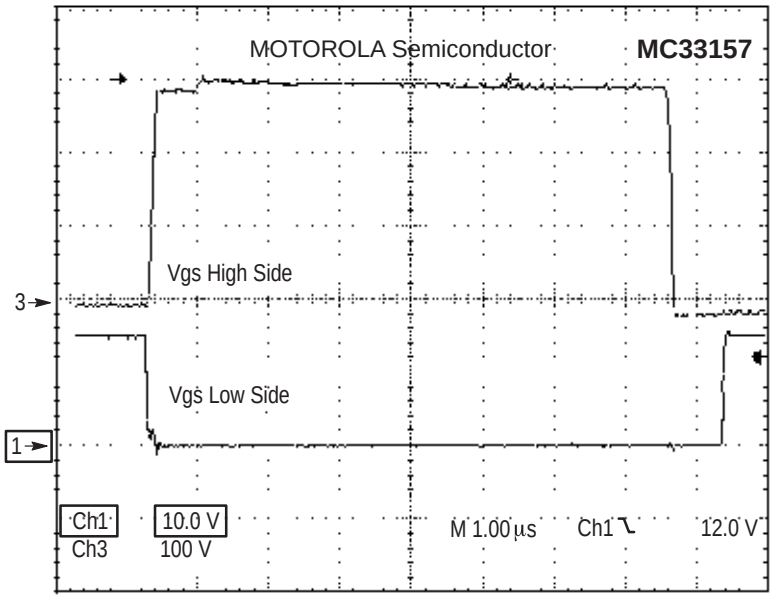


Figure 3.12 Typical Dead Time Under the Biases used in the Evaluation Board

LAMP STRIKE LOGIC

The internal comparator, associated to a built–in D type flip–flop, takes care of the detection of the lamp ignition state. The signal forced pin 9 can be either analog or digital as long as the pulse presents a positive slope followed by a negative slope, both being within the threshold as depicted in Figure 2.10.

Since heavy noise can be generated into the system, it is recommended to put a filter between pin 9 and the detection network. The evaluation board includes such a filter with a 10 kΩ resistor associated to a 10 nF capacitor to ground.

The state of the lamp can be detected by using a low cost circuit as depicted in Figure 3.13, any other topology being useable as long as they fulfill the trigger voltages defined in the data sheet.

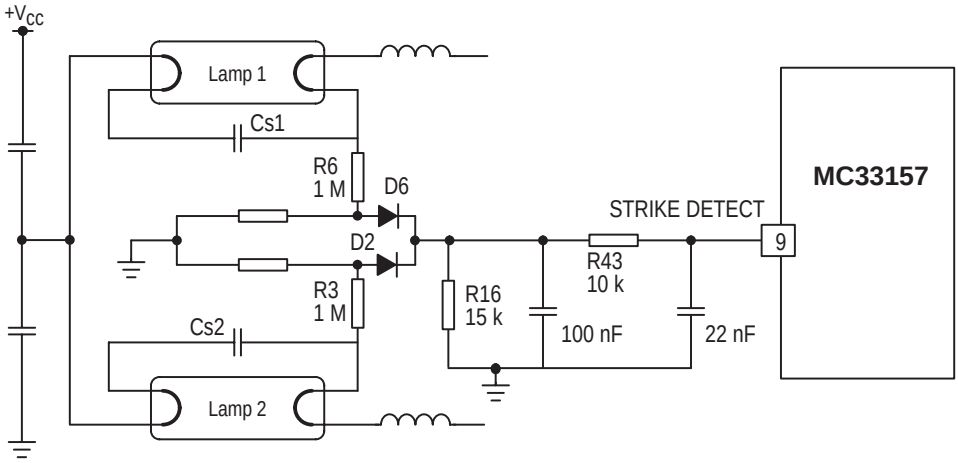


Figure 3.13 Basic Strike Detection Circuit

The analog gate built with D6/D13 senses the voltage across each lamp, providing the threshold voltages needed to trig the MC33157 internal logic as described here above. When the strike sequence is initialized, the high voltage across each resonant network generates a voltage at pin 9 higher than the 4.50 V expected by the internal comparator. When both lamps turn on, the voltage drops below the low threshold level (3.75 V) and the system jumps to the steady state mode. If either of the lamp does not strike, the voltage at pin 9 does not drop below 3.75 V and the MC33157 repeats the ignition sequence four time, then goes to a full stop if the lamp did not strike during any of these sequence. Of course, the designer can define a different strategy: the system might operate in steady state if one lamp is ignited only, depending upon the level defined by the voltage divider associated to the R16 node.

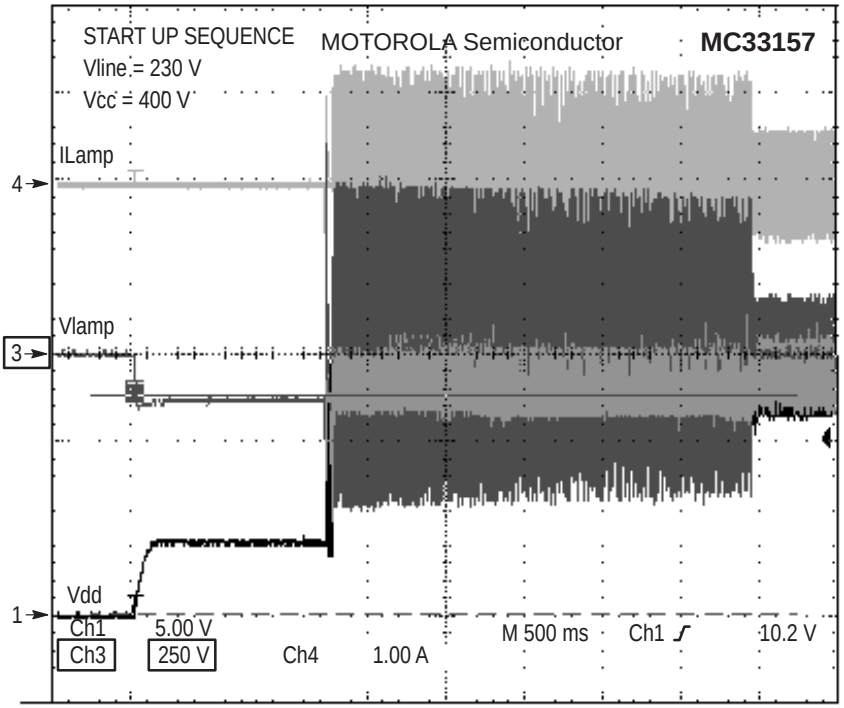


Figure 3.14 Typical Start–up Sequence Under Normal Operation

The strike detection input can be forced to a predetermined state by using a constant timing as depicted in Figure 3.15. This is useful for engineering purpose, or to run the device under different condition, without using extra component.

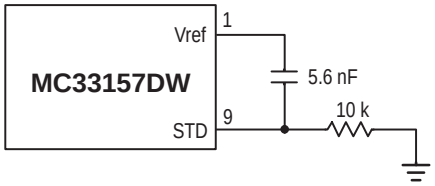


Figure 3.15 Force the Strike Detection Input

RE–LAMPING

The re–lamping function is achieved by using the RESET mode provided pin 10 of the MC33157 (see Figure 3.16). This logic input (CMOS compatible) turns off the converter, pulling both output MOSFET to zero gate voltage, when the voltage at pin 10 is zero. This is a non latched pin and the system resumes as soon as the voltage at RESET pin rises to one. When the RESET pin is released from zero, the system generates a frequency sweep and jumps to the steady state mode if the lamps are struck. In the event of a non strike detection, the cycle repeats four times, then goes to a full stop if either of the lamps do not ignite.

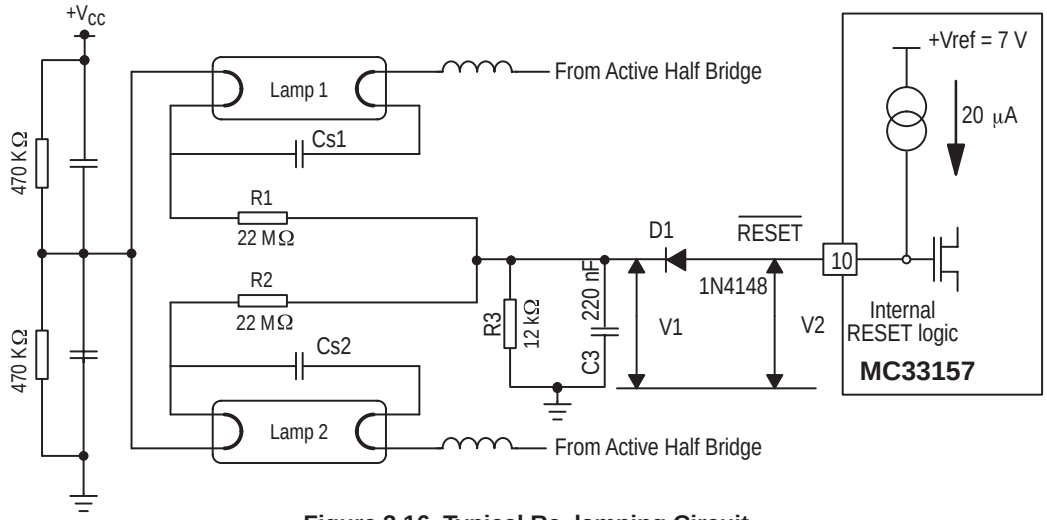


Figure 3.16 Typical Re–lamping Circuit

In order to maximize the flexibility of the MC33157, the RESET pin has a built in current source (20 μA) to force the internal circuit to a logic one if pin 10 if left open. This capability is used to implement an extremely low cost solution to control the re lamping function.

When both lamps are connected to the socket, the current coming from the Vcc/2 point through each filaments generates a DC voltage across the 12 kΩ resistor R3. On the other hand, the 20 μA current coming from the RESET pin adds to the same R3 resistor. Consequently, the DC voltage at pin 10 is higher than the 1.8 V zero logic level and the system operates under normal condition. If any of the lamp is disconnected, the voltage across R3 decreases, pulling pin 10 below 1.8 V and the system stops immediately (within 10 μs maximum). The system will automatically restart when a new lamp is connected to the socket as described here above. Diode D1 is mandatory to make sure that no negative going current will flow into the substrate of the IC under transient conditions.

Since the RESET pin is not latched, it is easy to built an OR gate at pin 10 to take care of other safety or goals one can define for the controller.

Moreover, since the system derives the low voltage energy from the output transformer of the PFC sub circuit, a one second period (depending upon start up resistor and reservoir capacitor at MC33262 Vdd pin) is automatically generated if there is a fault presents at RESET pin

START UP CURRENT

Since the start up current generates significant losses into the final module, several techniques have been used to improve this behavior. Among these alternatives, the solution depicted in Figure 3.17 provides a lot cost together with a nearly zero watt absorbed when the system runs in steady state.

When the line is switched ON, transistor Q4 supplies all the current to the MC33157, the Vdd voltage being regulated by zener diode D4. Resistor R5 is sized to handle the current absorbed by the IC, around 2.5 mA in steady state, and the one needed to drive two 8 A/500 V output MOSFET running at 60 kHz. Transistor Q4 is a MPSA44 with a BVCBO in extend of 500 V.

In the mean time, capacitor C1 is charged by resistor R1 until the voltage across pin 8 of the MC33262 reaches the UVON threshold (13 V typical). This delay time is defined by R1/C1, making sure that it extend the electronic ballast start up sequence timing (in the one second range).

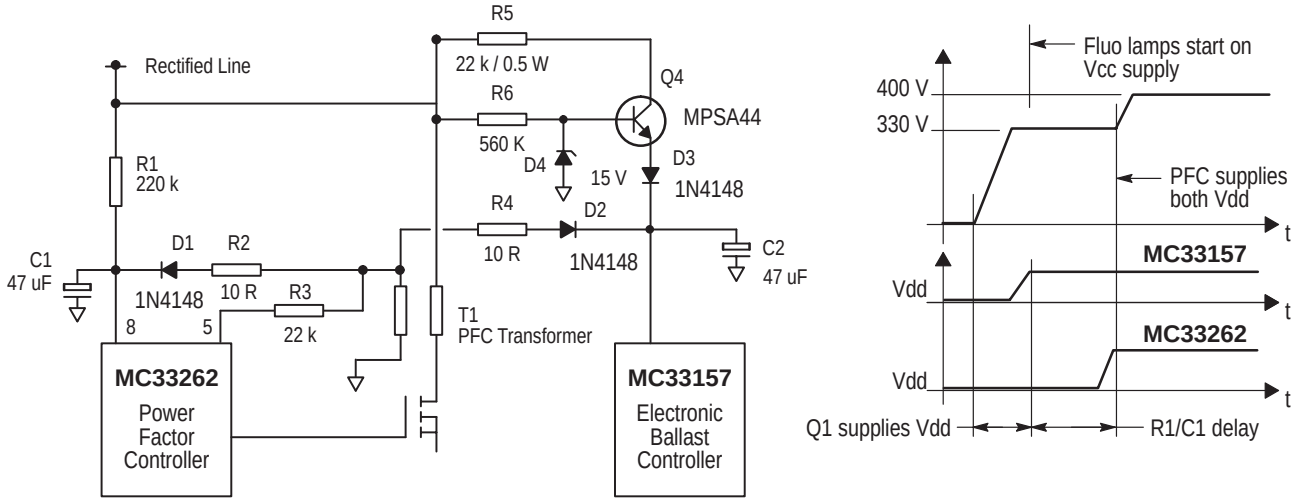


Figure 3.17 Typical Fast Start–up Power Circuit

At this moment, the PFC is activated and the low voltage is derived from the secondary of transformer T1. Note that, in any case, the secondary is necessary to synchronize the boost converter. Diodes D1 and D2 provide the rectification of the AC voltage and isolate the two IC chips Vdd one from the other. As soon as the voltage at pin 1 of the MC33157 becomes higher than the reference coming from zener D4, transistor Q4 turns OFF and the power dissipated into resistor R5 drops to zero. Consequently, there is no need to use a large wattage resistor since the start up time is limited to one second, eventually less, and the surface temperature of this resistor stays within the maximum rating for a carbon of metal film type of component.

Using a low cost 500 mW/5% resistor is large enough to handle the start up current, yielding a stable operation of the system.

To reduce the system cost, one can derive the PFC start–up supply from the line rectification and filtering as depicted in Figure 3.18. Since any industrial ballast uses a boost converter in the front end, it's possible to start the PFC chip first, the MC33157DW being powered later on by the secondary winding of transformer T1.

The medium value capacitor connected across the input bridge rectifier (C1) is rapidly charged at switch on and provides a path to smooth the line voltage: this is described in the MC33262 PFC data sheet. At this point, there are no supply coming from the mains to the ballast controller: consequently, this IC will not start until the front end is activated.

At this moment, the MC33157DW will get the energy from the PFC transformer auxiliary secondary. Let us now connect the input filtering to the reservoir capacitor connected across the Vdd pin 8 and ground of the PFC chip (C2). By using the right ratio between these two capacitors (say input cap is 680 nF, reservoir is 22 uF), we will very rapidly charge C2 up to 10 V (it takes around 1 ms). The rest of the Vdd supply comes from the standard low wattage resistor connected to the mains (82 k/0.250 W or 68 k/0.330 W) since we need to rise pin #1 up 13 V to turn on the chip.

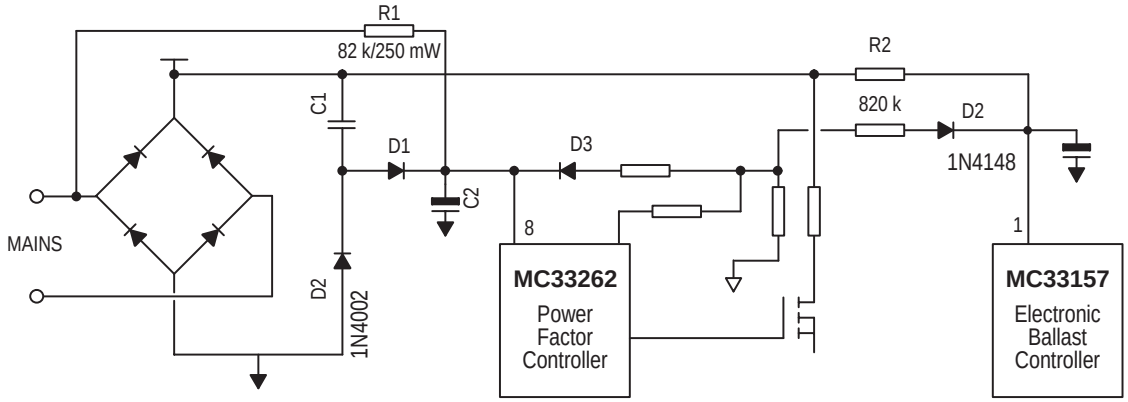


Figure 3.18 Low Current Start–up Circuit

Using this technique limits the delay time to 150 ms maximum to run the PFC chip. If the end user can accommodate a 330 mW, using a 68 k resistor will reduce this delay to less than 100 ms maximum. When the MC33262 is activated, the energy is transferred to the auxiliary winding and the MC33157DW can take as much as current is needed from this source. The ballast is powered within less than a couple of millisecond and the time needed to get the light out the lamp depends mainly of the preheating time defined for a given set of lamp. At the end of the day, the total sequence is well within the delay expected by the user when the mains is turned on.

The advantages of such an approach are:

- Integral Signal Conditioning
- There is no high wattage resistor used in the circuit.
- There is no external high voltage transistor; we save one MPSA44 and one zener.
- All used capacitors already exist in the module; there is no extra passive component.
- The auxiliary winding already exists to supply inductor demagnetization information and stand by supply for the peripheral circuits.
- This solution solves the 1.6 mA start–up current problem.

To make the system more efficient, a couple of low cost diodes (D1 and D2 1N4002 or equivalent) are implemented to make sure the high frequency current does not overheat the reservoir capacitor. Resistor R2 is recommended to avoid any latch up risk when the MC33157 is not activated (we might have pretty fast dV/dt here and uncontrolled operation can occurs). A module has been implemented with such a technique and has been proven stable in the MOTOROLA Toulouse laboratory.

Another alternative uses passive components only, making the cost at the bottom line, but a delay is generated as the electronic ballast controller is powered by the PFC transformer. Since this delay is depending upon the line voltage (ranging from 185 V to 255 V) and the R1/C1 time constant as described here above, the system cannot start the lamp within an accurate timing. The basic schematic is given in Figure 3.19, the evaluation board has been designed to accommodate either this solution or the one depicted in Figure 3.17.

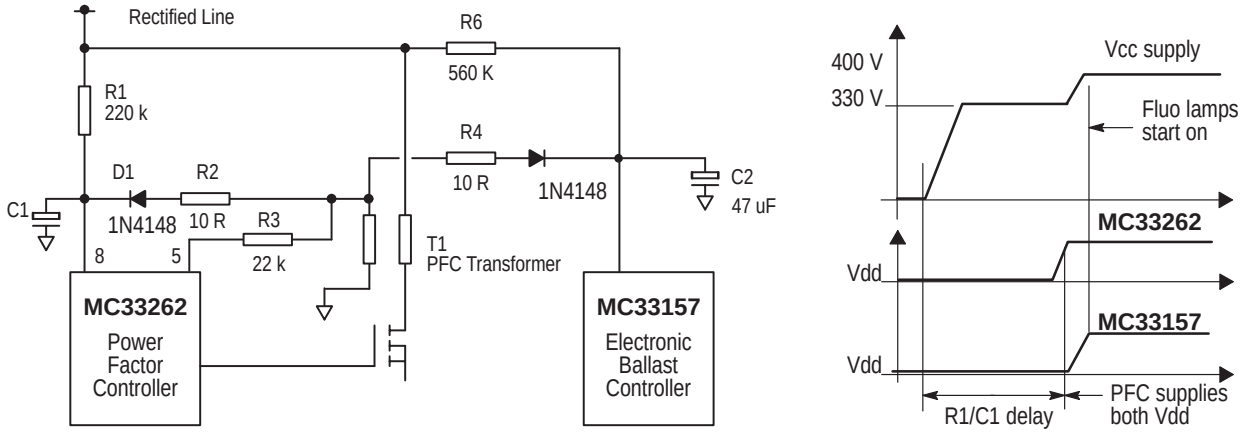


Figure 3.19 Typical Low Cost Start–up Circuit

Since the MC33157 Vdd input is zero until the PFC is activated, it is mandatory to force a minimum bias condition to avoid any risk coming from spurious pulse at any pins of this controller when the system operates as depicted in Figure 3.13. Resistor R6 fulfill this function by forcing approximately 3 V to Vdd/pin 1.

LOGIC AND ANALOG STATES

Although all the operating conditions are described in the Data Sheet, the table below provides a summary of the impact of every pin and biases to the MC33157 function.

Table 3.1 Logic and Analog States

	OPEN	SHORT GND	SHORT Vdd	CAPACITOR	RESISTOR	NOTES
Pin 3 CPH	No preheat. System jumps to FSWEEP.	Runs preheat continuously.	No preheat. System jumps to FSWEEP.	*Preheat timing activated*	If R> 330 k = system jumps to FSWEEP. If R< 330 k = system preheat continuously.	This pin is made flexible to run engineering tests during system development.
Pin 4 RSWP	Fsweep not stable. Not recommended.	System does not start.	Fpreheat unstable. Not recommended.	Fpreheat is F modulated.	*Normal operation*	See recommended range of operation.
Pin 5 CSWP	No Fsweep. Start up jumps straight from F1 to F2.	**NOT ALLOWED**	No Fsweep. Start up uses F1 only.	*Fsweep activated. Start up uses F1 to F2 modulation.*	No Fsweep. Start up jumps straight from F1 to F2.	Connecting pin 5 to ground will destroy the built–in Vref source.
Pin 6 COP	All clocks are cleared.	All clocks are cleared.	All clocks are cleared.	*All clocks are activated.*	All clocks are cleared.	See recommended range of operation.
Pin 7 IOP	No steady state clock.	No steady state clock.	No steady state clock.	*Steady state clock activated.*	No steady state clock.	See recommended range of operation.
Pin 8 DTA	Dtime = infinite	Dtime = zero	Dtime = infinite	Dtime = infinite after a delay.	*Dtime = valid*	It is recommended to make Dta > 10 k.
Pin 9 STD	System STOPS	System STOPS	System STOPS	System STOPS	System STOPS	*System is validated by a special pulse: see text.*
Pin 10 RESET	*Logic 1 System active*	Logic 0 System STOPS	Logic 1 System active	Create a RESET pulse with $t = (CV/I) \longrightarrow t = C*10^5$	If R> 100 k = Logic 1 If R <100 k = Logic 0	This pin can be used as an OR gate to cope with external logic.

Notes: Characters in *italic* indicate standard operation mode

Since a short to ground will definitively damage the circuit, pin 5 — CSWEEP — shall never be connected to a zero impedance node and cares must be observed to avoid such a situation.

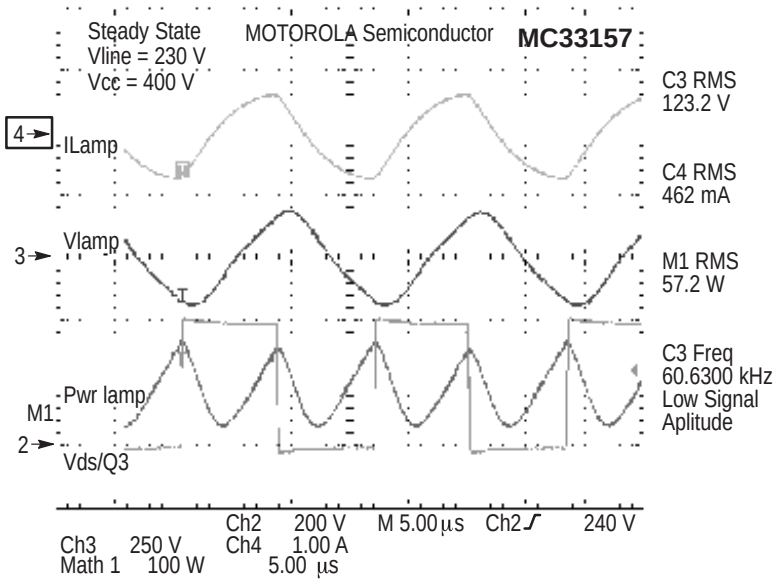


Figure 3.20 Typical Voltage and Current in One Lamp Under Nominal Steady State Operation

Table 3.2 gives the typical input power as a function of the ambient temperature, the system being monitored in a thermally controlled oven.

Table 3.2 Typical Input Power as a Function of the Ambient Temperature

Temperature	–20°C	0°C	+30°C	+50°C	+75°C	+85°C
Pin	93,73 W	92,24 W	90,20 W	89,37 W	87,34 W	86,9 W

Test condition: Vline = 230 V
Vcc = 400 V
Cos O > 0.97
Load = 2 x 55 W fluorescent lamp
No current feedback

These results demonstrate the stability of the MC33157: with +/– 4% variation over all the temperature range, the system is good enough to handle the industrial lamp ballast application without the need for an extra current loop regulation. Figure 3.21 gives the results coming from the evaluation board.

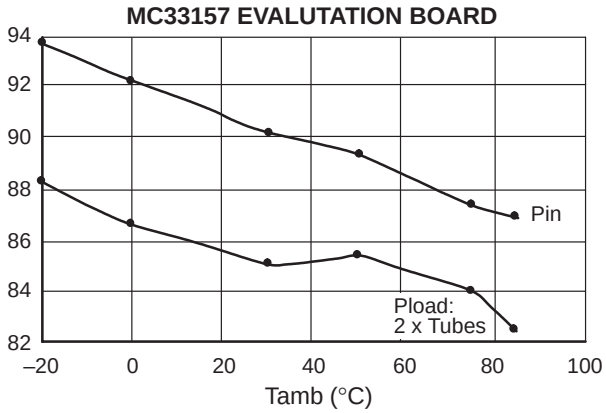


Figure 3.21 MC33157 Evaluation Board Global Efficiency at a Function of the Ambient Temperature

4 — ANNEXES

4.1 Since the passive components of the series resonant network have value tolerances, the designer must pay attention to the behavior of the RLC network as illustrated in Figure 4.1.

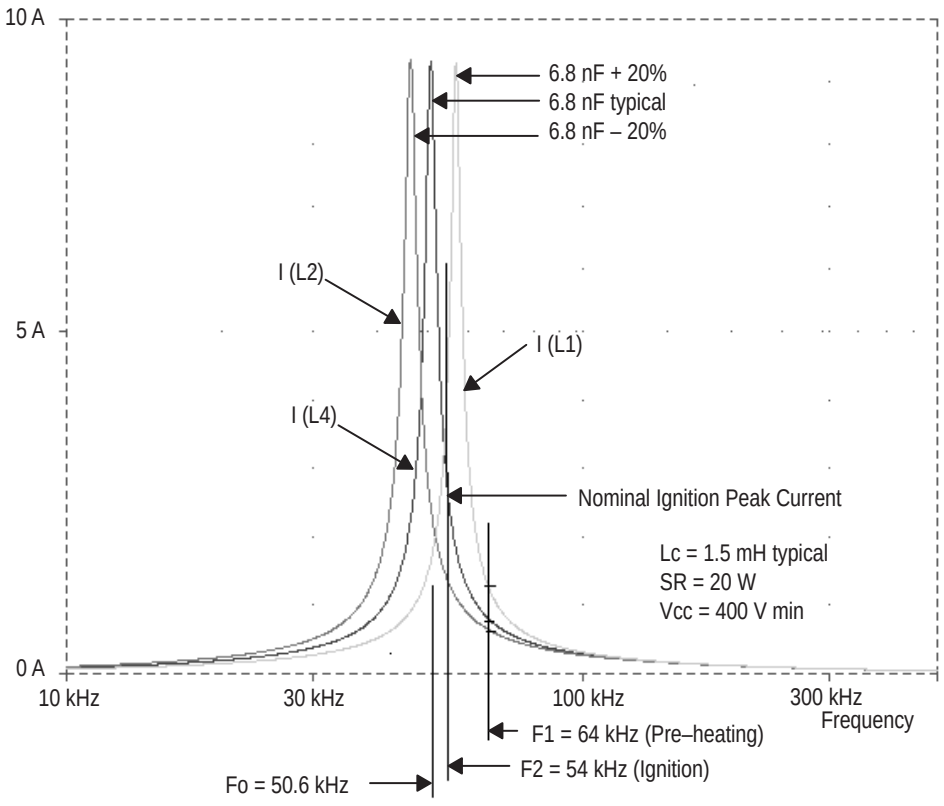


Figure 4.1 Resonant RLC Network Behavior as a Function of the Resonant Capacitor Tolerances

Fortunately, the tolerances of each components have a few risk to be at the same min or max values for a given module. This can be analyzed by running the Monte Carlo simulation tool to determine the worst case conditions.

4.2 Leaving aside the passive components tolerances and assuming, for the moment, the tube characteristic being constant, the output power is depending upon the operating frequency.

On the other hand, this frequency depends upon the tolerance of the reference voltage, particularly when the ambient temperature varies from the minus 20°C to the plus 85°C. The curve given in Figure 4.2 represents the behavior of the evaluation module under the here above defined conditions.

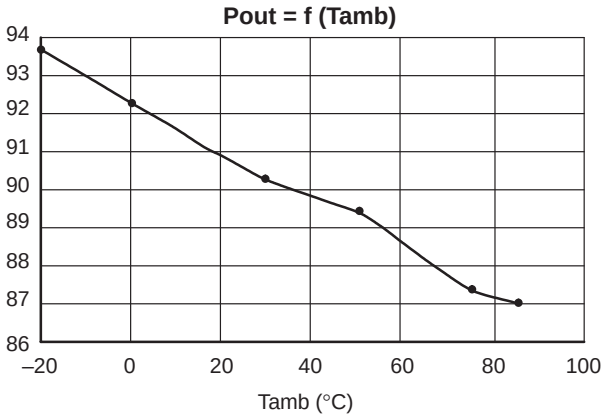


Figure 4.2 Pout = f (Tamb) at Fop = 58 kHz/Vcc = 400 V

With a global tolerance of +/– 3.5 % over the temperature range, the MC33157 makes possible the operation without any external feedback.

MAXIMUM dV/dt

Since the voltage transient is limited to 5kV/us, it is recommended to protect the device against extremely fast dV/dt. The most critical transient is developed when the system starts up from zero volt at Vdd (pin 1), the line being applied to the Vcc network. In this case, a very fast transient voltage exist between Vout (pin 15) and ground, and the controller can be forced into a latch up mode. Such very fast dV/dt, in the 10kV/us range, can be avoided by using the network depicted in Figure 4.3.

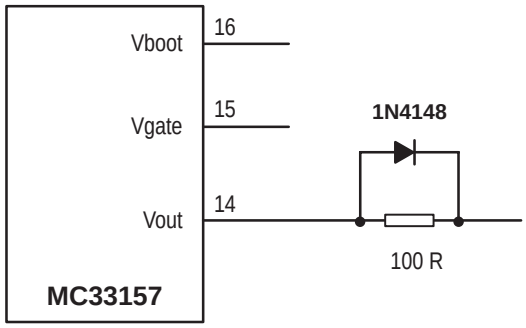


Figure 4.3 Protection of the MC33157 Against Extremely Fast dV/dt

CRITICAL COMPONENTS

Description	Value	Supplier	
Line Filter	2 x 27 mH/1.0A PN =	EUROINDUSTRIE ENC 11, rue des Herbiers 25190 NOIREFONTAINE FRANCE	Phone: (33) 381 99 39 30 Fax: (33) 381 99 39 31
Output L	1.4 mH PN = 575 22 007xx	VOGT 69, rue d'Aguesseau 92771 BOULOUGNE FRANCE	Phone: (33) 146 10 50 04 Fax: (33) 146 10 50 66
PFC Trans T1	PN = N2881–A Np = 300 uH	COILCRAFT 21 Napier Place Wardpark North CUMBERNAULD, Scotland G68 0LL – UK	Phone: (44) 1236 73 05 95 Fax: (44) 1236 73 06 27

EVALUATION BOARD COMPONENTS LIST

Index	Designator	Index	Designator
C1	47nF/630V	D1	1N4148
C10	220nF	D11	1N4148
C11	100nF 630V	D12	1N4148
C12	100nF 630V	D13	1N4148
C13	680nF/630V	D14	MR856
C14	100nF/450V	D15	1N4148
C15	100nF/450V	D16	1N4148
C16	1nF	D18	1N4148
C17	100nF	D2	1N4148
C18	100nF	D3	Vz15V
C2	1500pF/500V	D4	Vz14V
C20	6800pF/1000V/5%	D5	1N4148
C21	680nF	D6	1N4148
C22	100nF	D7	MUR160
C23	100nF	D8	BRIDGE 2A/800V
C24	6800pF/1000V/5%	D9	1N4148
C25	47uF/25V	F1	2A–TD FUSE
C26	22uF/450V	L1	1.4mH
C27	470pF/5%	L2	1.4mH
C28	100nF	L3	FILTER
C3	100nF	Q1	MTP8N50E
C30	47nF	Q2	MTP8N50E
C4	10nF	Q3	MTP8N50E
C5	100nF	Q4	MPSA44
C6	220nF	R27	22k/0.5W
C7	22uF/25V	R28	100k
C8	22nF	R29	82k
C9	100nF	R3	1M
R1	22R	R30	2.2M
R10	470k	R31	100k
R11	470k	R32	100k
R12	22k	R33	100R
R13	100k	R34	330k
R14	0R	R35	330k/0.5W
R15	2.2M	R36	820k
R16	15k	R37	10k
R17	0R	R4	33k
R18	0R	R5	33k
R19	100k	R6	1M
R2	22R	R7	22k
R20	820k	R8	10R
R21	1.2M	R9	Not Used
R22	330R	T1	N2881–A

Index	Designator	Index	Designator
R23	0.47R/2W	TUBE 1	FLUO_TUBE
R24	12k	TUBE 2	FLUO_TUBE
R25	1.5M	U1	MC34262DW
R26	10R	U2	MC33157DW

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