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Plastic Ball Grid Array (PBGA)

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INTRODUCTION TO THE PBGA

The Plastic Ball Grid Array or PBGA package is the industry description of what is sometimes referred to as Motorola's OverMolded Pad Array Carrier or OMPAC package. It was developed by Motorola in the late 1980's for use in Motorola products with space limitations such as radios, pagers and cellular telephones. Since that time it has grown in popularity within the electronic industry and standard body sizes and pin counts have been adopted by JEDEC and soon by EIAJ. The many benefits of using PBGA over similar lead count leaded devices include:

1. Board space efficiency.
2. Thermal and electrical performance and ease of enhancing both.
3. Excellent surface mount yields when compared to fine pitch leaded devices.
4. Lower profile (i.e., overall thickness).
5. Almost unlimited pin count capability.
6. Compatibility with existing surface mount, test and handling equipment.
7. Potential lower total cost of ownership compared to leaded devices due to reduced scrap, rework and lack of need for fine pitch assembly equipment.

This application note serves to provide general information about the PBGA package as well as provide information about its implementation into products and surface mount assembly.

PACKAGE CONSTRUCTION

The PBGA package is based on a printed circuit board (PCB) substrate or "leadframe" fabricated of Bismaleimide Triazine (BT) epoxy/glass laminate. This material is used over standard and multi-functional FR4 laminates for its high glass transition temperature of 170 – 215°C and heat resistance (230°C exposure for 30 minutes with no degradation). The standard core thickness of this two layer substrate is typically 0.2 mm with 18 μm (half ounce or 0.7 mil) copper on each side. A two mil thick (thickness over epoxy glass) dry or dual pass wet film soldermask is currently used to ensure that all the substrate vias will be completely tented. The silicon chip containing an integrated circuit is die bonded to the top side of the substrate using silver-filled epoxy typical of that found in leaded devices. The chip is then gold wire-bonded to wire bond pads on the circuitized substrate. Traces from the wire bond pads take the signals to vias which carry them to the bottom side of the substrate and then to circular solder pads. The bottomside solder pads are laid out on a square or rectangular grid with either a constant 1.5 mm or 1.27 mm pitch. These two pitches, as well as a 1.0 mm pitch, are prescribed by the JEDEC registration for PBGA which is included in Appendix A. An overmold (or possibly a liquid or "glob-top" encapsulation) is then performed to completely cover the chip, wires and substrate wire bond pads. Typical feature dimensions common to most PBGA configurations, as discussed above, are summarized in Table 1.

Individual preformed 30 mil diameter solder balls are gang dipped in no-clean paste flux using a specially designed pick-up tool then placed on each bottomside solder pad using an internal Motorola developed (by Motorola Manufacturing Systems in Boyton Beach, Florida), but commercially available, robotic bumping cell. To provide somewhat greater fatigue resistance and a finer, more homogeneous solder microstructure, the near-eutectic (62%Sn/36%Pb) solder balls also contain 2% Ag, which results in a solidus temperature of 179°C. The balls are then reflowed onto the solder pads using a conventional forced convection nitrogen reflow oven and a typical surface mount assembly profile with a maximum specified temperature of 230°C. Following reflow, the substrates are centrifugally cleaned in Terpene (CFC-free organic cleaner) to remove flux residue as well as any fibers and particulates from the remainder of the package.

The entire process described above, takes place on a substrate containing several (currently from three to six) PBGA devices. The final step in assembly is the singulation or excise of the individual PBGA devices out of that larger substrate or panel. The resulting device has a body size that now conforms to JEDEC standards, although for the near term some pre-JEDEC devices are included in Motorola's package offerings. The package outline dimensions for several PBGA configurations (86, 119, 169, 225, and 357 pins) currently offered by Motorola are included in Appendix B. The total number of I/Os on the package is obviously determined by the body size and pitch. Additionally, the JEDEC standard allows for any number of balls to be depopulated from a completely populated matrix (i.e, staggered pitch or center balls depopulated). A cross-sectional rendering of a device mounted to a PCB is pictured in Figure 1.

Table 2 provides nominal room temperature values for the physical properties of all the materials that comprise the PBGA package. It is important to note that the properties of many of the PBGA materials have a temperature-dependence that is not included in the table.

Table 1. Typical Nominal Dimensions of Selected PBGA Substrate Features

Feature	Dimension (mil/mm)	Comment
Substrate Thickness (Two Layer)	7.9/0.20 14.1/0.36	BT/glass laminate core thickness. Overall (BT/glass + Cu + soldermask).
Substrate Thickness (Four Layer)	15.7/0.40 24.0/0.60	BT/glass laminate core thickness. Overall (BT/glass + Cu + soldermask).
Copper Thickness	0.71/0.018 1.2/0.030	Clad to BT/glass laminate. Plated on (electroless + electrolytic).
Trace/Space Widths	3.5/0.090	Minimum.
Soldermask Thickness	2/0.05 1.2/0.03	Over BT/glass. Over copper features.
Via ϕ	9.8/0.25 15.7/0.40	Typical Minimum. Normal.
Solder Pad Cu ϕ	35/0.89 30/0.76	Standard. Specific 1.27 mm pitch devices.
Soldermask Opening ϕ	25/0.64 22/0.56	Standard. Specific 1.27 mm pitch devices.

NOTE: ϕ = Diameter. All dimensions are approximate and are for reference only.

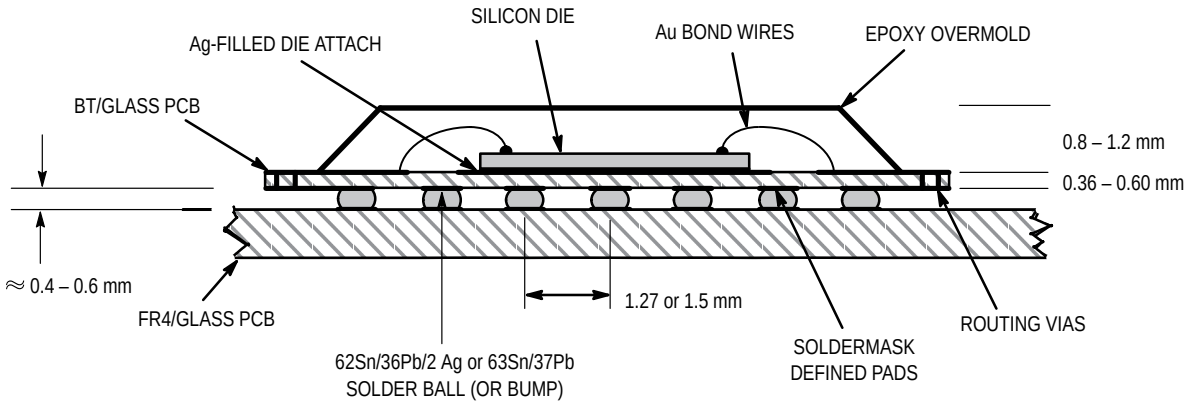

Figure 1. Cross-Sectional View of an PBGA Mounted to a PCB

Table 2. Physical Properties of All Materials Used in the PBGA Package at 23°C

Material	Elastic Modulus (ksi)	Poisson's Ratio (--)	T_g (°C)	CTE – x, y/z < T_g (ppm/°C)	Thermal Cond. (W/m-°K)
Copper (ED/Rolled)	17,500	0.345	1085 (melt)	17	418
62% Sn/36% Pb/2% Ag Solder	4,600	0.4	178 (melt)	21	50
Dry Film soldermask	300	0.45	≈120	50	0.33
BT/Glass Subtrate	2,760	0.195	170 – 230	15/57	0.19
Silicon Die	18,900	0.278	1412 (melt)	2.6	83
Mold Compound	2,200	0.25	196	15	0.67
Ag Filled Epoxy Die Attach	1,070	0.3	77	52	1.38

MOTHERBOARD LAYOUT

The PBGA package, with its leads or balls in an array configuration, presents some unique challenges to overcome with respect to motherboard routing when compared to peripherally leaded devices. Additionally, the volume of solder in the joint is relatively large and since all of it is molten during reflow, special considerations must be taken when determining appropriate pad geometries.

FOOTPRINT GEOMETRY

A solderable surface defined by soldermask, also called a soldermask defined (SMD) pad, has traditionally been used and recommended by Motorola for the PBGA. This is because the soldermask defined pad provides better adhesion strength to the PCB. This greater adhesion comes from the fact that the copper pad diameter is greater than that of the soldermask opening with the overlapping soldermask providing added strength. Since the strength and compliance of solder balls is far less than that of leads, the copper pad/FR4 laminate adhesion becomes a relatively weaker link than with leaded devices. This extra strength could be important in certain extreme bending and high thermal mismatch-induced stress situations (i.e., large package or die, large and rapid temperature swings).

The diameter of the solderable surface is generally chosen to match that on the PBGA. The standard PBGA soldermask opening is specified at 25 mils for all 1.5 mm pitch devices. As the pitch is reduced to 1.27 mm and the package substrate routing becomes more difficult, some devices have required reducing the soldermask opening and copper pad diameters to a specified 23 and 31 mils, respectively. The copper pad diameter is chosen to allow for the worst case soldermask to artwork misregistration that may be encountered. For the majority of PCB fabricators the tolerance on that misregistration is from $\pm$ 2 to $\pm$ 4 mils and can be as much as $\pm$ 5. Likewise, the soldermask opening has some dimensional variation from overdeveloping and aperture diameter changes to compensate for the same. The tolerance on the soldermask opening should be chosen such that its diameter is never less than that on the PBGA. Having a joint with a larger diameter at the device than at the board may cause it to be more unstable while molten and increase any risk of shorting. Therefore, it may be advantageous, for example, to specify an opening with a 26 mil nominal diameter in the case of a PCB supplier who can guarantee a $\pm$ 1 mil tolerance. Figures 2a to 2c give examples of various soldermask defined pads, one of which (Figure 2a) is shown with some possible dimensions. The various routing trade-offs associated with different pads for 1.27 and 1.5 mm pitch packages will be discussed later.

The individual pad geometry also has to incorporate the desired escape method to be used between routing to other board layers with vias or simply routing on the device layer (or typically, a combination). The pads shown in Figures 2a and 2b have integral vias to take the signal immediately to another layer while the Figure 2c and 2d pads have traces exiting them which keep the signal on the component layer. The connection between the via and adjacent via pad can either be with a trace (which forms what is referred to as a dumbbell or dogbone pad) or by simply filling in the entire area between the via pad and solder pad to form a teardrop pad.

Another integral via geometry technique that has been tried is to put a via concentric to the pad or via-in-pad (VIP). Special consideration must be taken with this configuration with regard to the volume of the via and its “thieving” of solder from the joint which results in a much lower device stand-off. Ways to get around this problem are to compensate by screen printing extra solder paste, tent the via with copper, use the minimal cost-effective via diameter possible and/or request completely solder filled vias from the PCB fabricator. It should be stressed that only minimal data exists as to the reliability and processibility of the VIP configuration and it is only mentioned here as an option that requires further investigation.

Non-soldermask (NSMD) or copper defined pads, as shown in Figure 2d, pads have also been used successfully with the PBGA. In this case there is a soldermask clearance area around the copper pad. Due to the large volume of solder present in the PBGA ball, the solder will wet down the sides of the pad in the case of a non-soldermask defined pad. This will result in an effectively greater diameter joint and lower accompanying stand-off (see Figure 3). This lower stand–off can result in a reduced attachment reliability in accelerated thermal cycling.The same considerations as mentioned above with regard to soldermask to artwork registration tolerances have to be applied to a non-soldermask defined pad in determining the diameter of the soldermask opening so that it does not touch or exhibit tangency to the copper pad. In determining which pad to ultimately use, the application environment, the desired board technology/ cost, and the assembly characteristics need to be taken into account.

ESCAPE ROUTING

The main perceived drawback of using BGA is the challenge of routing all the required signal, power and ground pins to the system board without increasing printed circuit board (PCB) complexity and therefore cost. Fortunately, this challenge is easily overcome by Motorola with thoughtful package pin assignment and device configuration considerations (pitch, ball count, ball depopulation methods) in conjunction with the choice of solder pad geometry and board technology (number of layers and line/space widths). If signal pin assignments are made too deeply within the BGA matrix, board level escape using conventional eight mil printed circuit board fabrication technology becomes difficult for large matrices. Current PCB technology with eight mil lines and eight mil spaces typically does not incur any additional cost. For this reason Motorola attempts to perform signal pin assignment such that the outer four rows of the PBGA contain all the signals that must be escaped. The Motorola 68356 chip is an example of such a properly assigned BGA footprint that provides users with easy board–level escape with no cost adders for sub–eight mil line and space board technology or internal signal layers. The 68356 is a Signal Processing Communications Engine with integrated functions such as a 68000 based microprocessor, RISC communications core, 24 bit DSP and a PCMCIA controller. The device is housed in a 25 mm PBGA, using a 1.27 mm or 50.0 mil ball pitch. The balls are in a 19x19 array with the four corner balls depopulated to result in 357 pins.

One of the key features that facilitates the routeability of this package is the location of the power and ground assignments to an 11x11 matrix in the center of the package. Within

this inner matrix, the centermost 9x9 pins form a ground bus and the remaining 40 pins encircle that with what is called a power ring. Those power and ground pins do not need to be escaped as they are dropped straight down using dumbbell or teardrop shaped pads with offset vias to the associated power and ground planes on the circuit board. This leaves the outer four rows containing 236 signal pins around the perimeter of the package that need to be escaped. This package itself has 23 mil diameter solder pads on it and the same solderable surface diameter or only slightly larger is recommended for the PCB. Therefore, using a 23 mil non–solder-mask defined pad in conjunction with a 25 mil diameter via pad a board employing eight mil lines and spaces can be used to easily route these four outer rows using two signal layers. The escape routing of the outer two rows can be achieved on the topside of the PCB without using vias and the third and fourth rows from the outside are escaped by dropping down vias and escaping on the bottomside. This example is illustrated in Appendix C, which shows a representative top and bottomside signal layer routing schematic for the 68356.

A similar package design methodology is used on other devices packaged in BGA such as Fast Static RAM devices that utilize a 7x17 and soon a 9x17 array PBGA, the PowerPC 603™, PowerPC 604™ microprocessors as well as the MPC105 PCI Bridge/Memory Controller for PowerPC™ microprocessors that will be available in a ceramic BGA. The fact that this 119 pin FSRAM package only contains seven rows in one direction further simplifies routing since there are a maximum of three buried rows. As can be seen in Table 3, no matter what geometry (diameter and SMD versus NSMD pad configuration) is chosen for 1.5 mm pitch PBGA devices one eight mil trace can always be routed between two solder pads. Only if NSMD pads are used an eight mil trace can be routed between two pads at 1.27 mm pitch. As can be seen in Table 3, a maximum trace width of six mils would be needed to use an SMD pad.

As PBGA pin count and matrix size increase it may be necessary to make signal assignments on more than just the four outer rows. This would require more that one buried row on each of the outer layers to be escaped on a given PCB layer to maintain a two signal layer board. When this becomes the case, trace size will have to decrease further from the standard eight to six. Table 3 also shows how many traces can be routed between two pads for given line and space technologies down to three and three and all the current standard PBGA pad diameters. For example, when and if it becomes necessary to route two signal traces between NSMD pads at 1.27 mm pitch, five mil trace widths will be necessary to avoid adding extra signal layers. If SMD pads were used those traces could only be three mils wide maximum. This example once again underscores the routing advantages of NSMD pads.

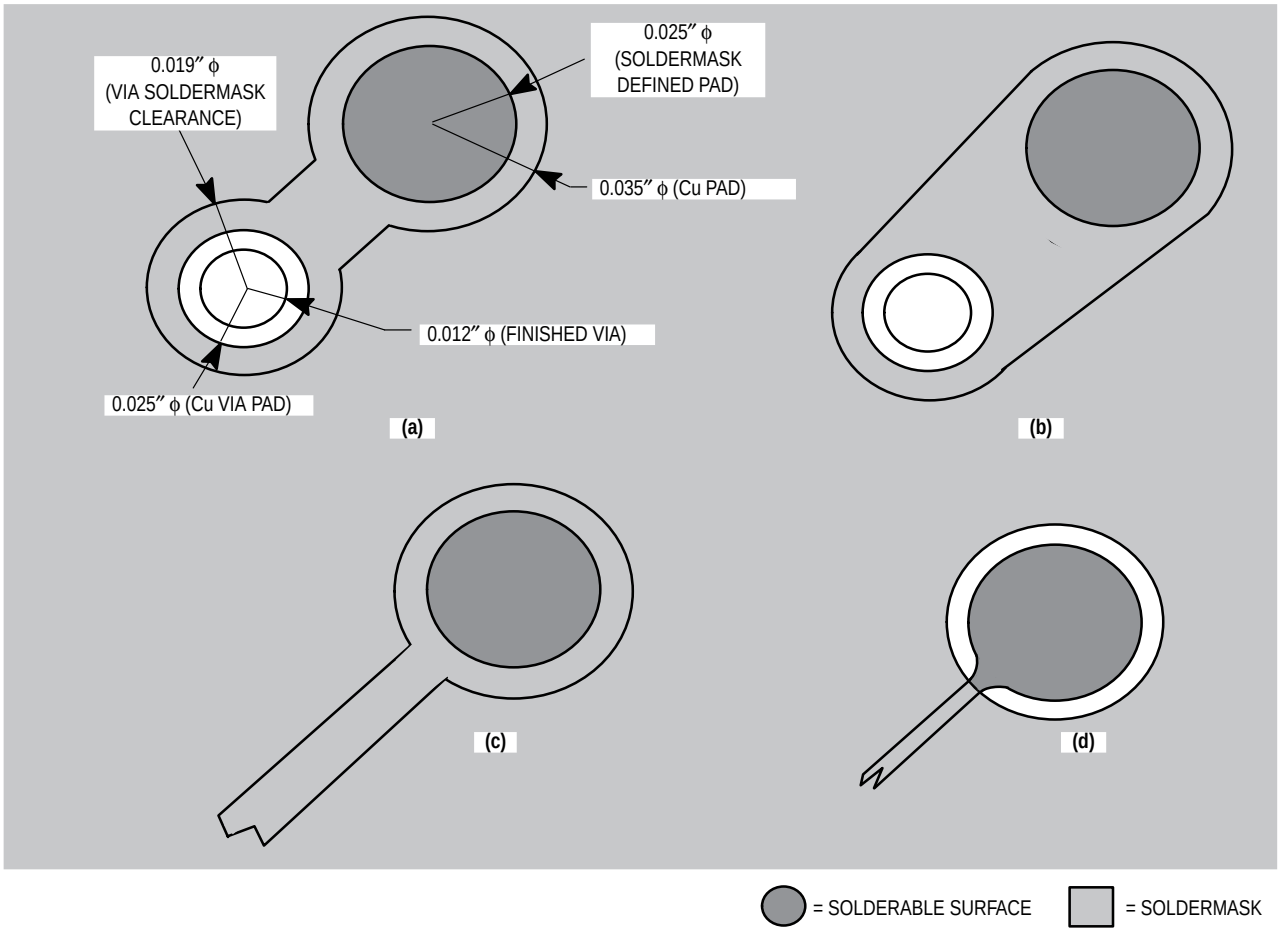

Figure 2. Pad Options for PBGA Motherboard Routing: a) Dumbbell pad shown with typical dimensions, b) Teardrop, c) No integral via for escaping onto top layer, d) PBGA version of standard surface mount pad with soldermask clearance around the solder pad.

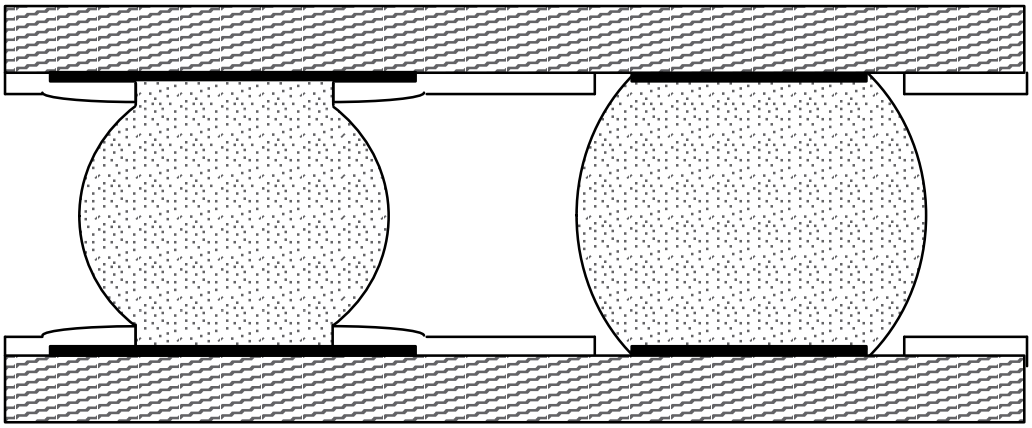

Figure 3. Comparison of PBGA Solder Joints with: a) soldermask-defined pad and b) conventional non-soldermask defined pad. Note the greater volume of solder and greater effective joint diameter for the non-soldermask defined pad to achieve the same stand-off.

Table 3. Number of Escape Traces That Can Be Routed Between PBGA Pads Given Device Pitch, Pad Diameter, and Board Line/Space Widths

Board Technology (Line/Space Widths in Mils)	Number of Escape Traces Routed Between Pads Given Ball Pitch and Pad Diameter in (mms/mils). Shaded Columns Represent NSMD Pads.							
	1.5/23	1.5/25	1.5/31	1.5/35	1.27/23	1.5/25	1.27/31	1.27/35
3/3	5	5	4	3	5	3	2	2
4/4	4	3	3	2	2	2	1	1
5/5	3	2	2	1	2	2	1	1
6/6	2	2	1	1	1	1	1	
8/8	1	1	1	1	1	1		

Note: When encountered, fractions of traces were rounded down.

SURFACE MOUNT ASSEMBLY

One of the greatest advantages of the PBGA package is that it can typically be placed onto printed circuit boards and assembled using existing surface mount equipment. This is not true for many other new and high pin count packaging technologies such as TAB, DCA, fine pitch QFPs, PGA, etc. Most require new or upgraded process equipment and in some cases new processes or manual assembly. It has the added advantage of being completely compatible with existing handling systems. Open tooled handling media, namely trays and tape and reel (heat seal or C-pak) are available for many of the JEDEC PBGA body sizes. Handling damage is significantly reduced by package robustness due to the absence of fragile leads.

FLUXING

Either solder paste (cream), paste flux or liquid flux (i.e., spraying, dispensing, or foaming) must be applied to the PC board solder pads prior to assembly. This is necessary to not only reduce oxides formed on the solder pad, but also on the solder ball. Slight solder ball oxidation may occur during exposure to burn-in, storage, and dry baking in non-inert atmospheres. Typically, the method chosen to apply flux is done to maintain compatibility with current processes. Due to the fact that the solder ball is comprised of eutectic or near-eutectic solder and its entire volume is molten during reflow, it is not necessary to add solder volume to the joint with solder paste. The 30 mil diameter ball provides enough volume to give an 18 to 24 mil average stand-off across the device depending on package and device/board solder pad configuration. This is typically enough stand-off to ensure that no opens will occur due to device or board warpage at elevated temperatures (more discussion on device warpage in the Coplanarity section). Applying an amount of solder paste equal to 14% of the ball volume (i.e., eight mil stencil, 25 mil diameter apertures, final solder volume = 1/2 solder paste volume) will generally increase the stand-off by one to two mils. In some cases additional solder volume may be advantageous to increase stand-off and subsequent device solder joint reliability. However, applying larger amounts of solder paste with the use of thicker stencils and/or larger apertures has the potential to result in joint voiding, especially when combined with fast oven ramp rates and volatile fluxes. Voids are formed when flux volatilizes and is entrapped within the joint. Voids form at the bottom (motherboard interface) of the ball, but end up at the joint/package interface due to buoyancy effects. These voids have been shown not to be a reliability risk. Figure 4 shows a pad from an PBGA test board with eight mils of solder paste screenprinted onto it prior to device

placement. Besides screening solder paste, pin transfer and single point dispense of paste flux have also been used successfully on PBGA within Motorola.

DEVICE PLACEMENT

Due to the large pitches involved relative to fine pitch QFPs, pick and place is much simpler and involves lower required machine accuracies and resolutions. Additionally, due to tight ball pattern to device edge tolerances (better than ± 3 mils) relative to the pitch, placement can be performed off of the body outline. This is the method currently used for much smaller devices in the industry using extremely fast "chip-shooters". Additionally, new equipment with upward looking vision or lasers (dual lasers or better are recommended over a single laser system) that are specifically designed for the ball grid array are becoming available. This equipment centers off the ball array itself and can also check for missing balls and in some cases calculate device coplanarity real-time. Finally, due to the fact that the PBGA is self-centering in the reflow process, a device can be placed up to 50% off pad and still be expected to align itself. The self-centering feature, which is a result of the surface tension of the molten solder, can be easily observed by placing devices deliberately off pad and reflowing.

REFLOW

Surface mount reflow of the PBGA device is similar to that of leaded devices. The process of reflowing a PBGA is sometimes referred to as a Controlled Chip Carrier Collapse Connection or C5 since the solder ball starts with an approximate height of 25 mils (plus paste if any) and collapses down three to seven mils during reflow due to the weight of the package and wetting of the motherboard pad. Devices have been reflowed successfully in IR, convection and mixed heating ovens as well as with vapor phase. Care must obviously be taken that each solder joint is exposed to the solder solidus temperature immediately following a flux-dependent high temperature soak period in which the flux is mobile and active. An example of an IR reflow profile (not optimized) obtained by placing thermocouples under two different devices at the middle and corner of a 4.5″ x 7.5″ four layer test board is presented in Figure 5. The main difference in reflowing the PBGA lies in the fact that the joints are heated more from the package and board as opposed to direct air impingement or IR exposure onto the leads. It is relatively easy to obtain a suitable profile with boards containing a variety of surface mount and through-hole device types along with the PBGA.

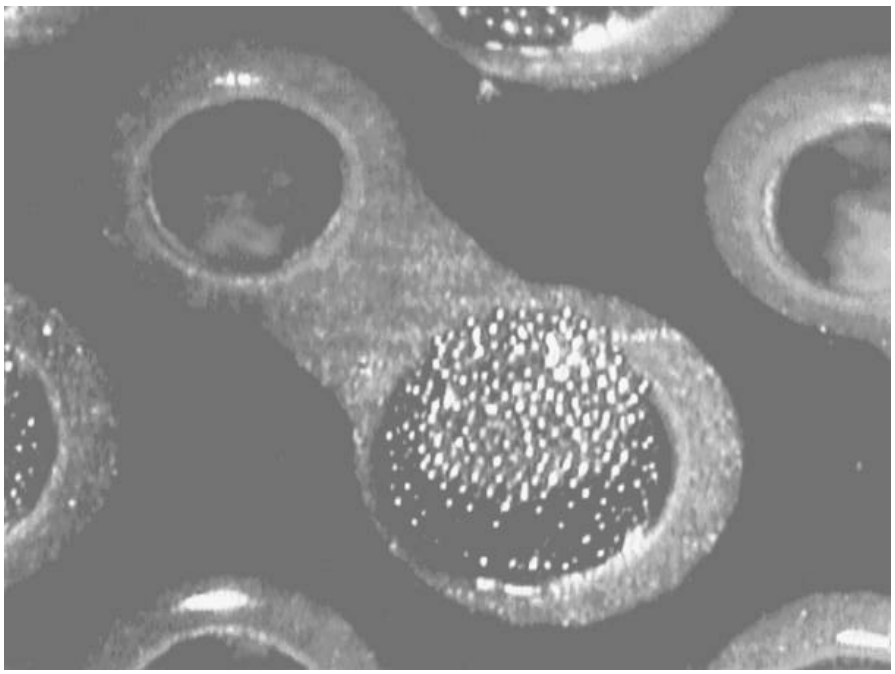

Figure 4. Micrograph of an PBGA Test Board Pad with Eight Mils of Screenprinted Solder Paste (Magnification of Approximately 40X, 45°)

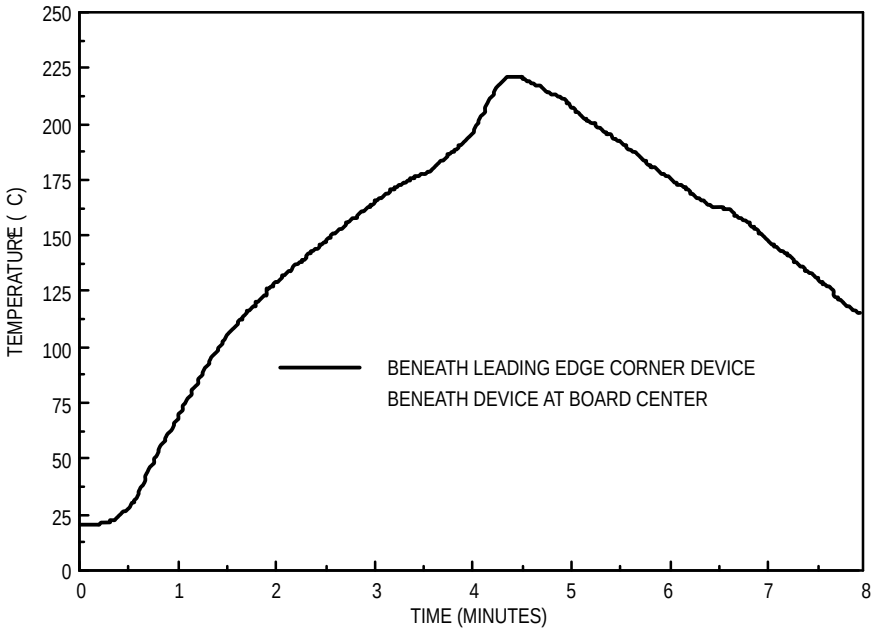

Figure 5. PBGA IR Reflow Profile Obtained by Placing TCs Underneath Devices

Another difference between PBGA and typical leaded devices is in profiling. The profiling thermocouple(s) (TC) must be placed underneath the package and preferably within an actual solder joint. This requires using thinner TC wire than may typically be used as to allow the device to solder to the board almost normally with minimal tilt or non-contacting balls. A suggested procedure for making a profile board is to solder the TC bead to a ball under the device. The center ball is recommended since it is likely to exhibit the minimum peak temperature and is therefore the worst-case position for a cold solder joint. It is advantageous to also TC the outermost ball on the leading edge of the device to obtain worst case maximum temperatures. The device is then hand placed onto a prefluxed board footprint, secured with the minimal amount of polyimide (i.e., Kapton™) tape possible and reflowed. The tape is then removed and the board can be used for repeated profiles, assuming the TC did not break free and that the device reflowed somewhat normally onto the board. An alternate way of more securely fastening a TC is to remove a PBGA ball with a solder sucker or wick and to attach the bead to the site using high-temperature solder or thermally conductive epoxy. Drilling a hole through either the top of the device or the bottom of the board for subsequent thermocouple placement can also be done successfully. Also, inserting a TC with thermal grease on the bead under an already mounted package can sometimes yield sufficient results.

COPLANARITY

The JEDEC standard for maximum allowable noncoplanarity is currently 0.15 mm (5.91 mils), regardless of package size or pin count. This coplanarity is defined in the standard as the maximum distance from the highest ball to a seating plane formed by the three balls that the package would rest on if placed on a perfectly flat surface. Any lack of PBGA coplanarity is a result of two elements, the warpage of the overmolded substrate and differential substrate pad to-solder ball tip heights. The substrate warpage is typically the major contributor to any lack of coplanarity, while the solder ball heights are relatively uniform. At room temperature, the typical PBGA has a slight upward curvature, such that 225 pin PBGAs with a 27 mm body size have been measured to have a worst case coplanarity of around four mils.

Determining the coplanarity per the JEDEC standard requires scanning all the PBGA bumps and determining the relative positions of their tips in space. Software that takes into account the center of mass of the part must then determine which three balls the device would rest on and the distance from the remaining ball tips to a plane formed by these three seating balls. An automated system, the Model 830B, to do this has been developed by View Engineering and is available now (priced in the mid-$100K range). The system also has the capability to determine the coplanarity to a best fit plane, ball volumes, the absence of balls and the deviation of ball tips from the expected x-y grid. A more expensive and flexible system that also performs printed solder paste height inspection is also available from Synthetic Vision Systems, who are affiliated with View. Among others, RVSI is also a potential equipment supplier.

SOLDER JOINT INSPECTION

One of the perceived drawbacks to using PBGA technology is the fact that, as with any array package, the interior joints are not visible to be readily inspected. Perimeter joints, can be readily inspected. High volume users have presented data showing that the 169 and 225 pin PBGA has one to two orders of magnitude fewer solder-related defects that the 208 PQFP.

X–ray inspection is typically used during assembly process development and for failure analysis. Due to the atomic density of the lead in the solder joints, standard resolution real-time x-ray systems may only be useful in determining shorts and missing or double balls, which are readily observable (see Figure 6). More subtle joint assembly defects like voids, total wetting of the motherboard pad (i.e., full or partial opens) and solder splattering/balling require more sophisticated systems to detect. Very costly x-ray laminography systems (i.e., Four Pi Systems) can detect such features,

although their current cost and image acquisition cycle time may be prohibitive for some users. Fein Focus and Imaging Systems International (affiliated with Nicolet) have both developed lower cost systems with the resolution to identify voids and in some cases non-contact failures. Examples imaged with the Fein Focus Model FXS-160.32 and Nicolet Model NXR-1400, are presented in Figures 7 and 8, respectively. Other systems with similar capabilities are available from Lixi, I.R.T. and others.

A pad geometry design change that can allow detection of non-contact failures or opens involves modifying the motherboard pad footprint. A tab or ear is placed in the soldermask defined pad as in Figure 9. During reflow, solder fills the pad and is readily observed by using even inexpensive x-ray systems. If solder plated or HASL motherboards are used or solder paste is screened on prior to reflow, this ear would already be filled with some solder. In these cases, the x-ray would have to be of sufficient resolution to distinguish between an ear filled by solder from the ball and one already filled by plated, HASL'd or stenciled on solder.

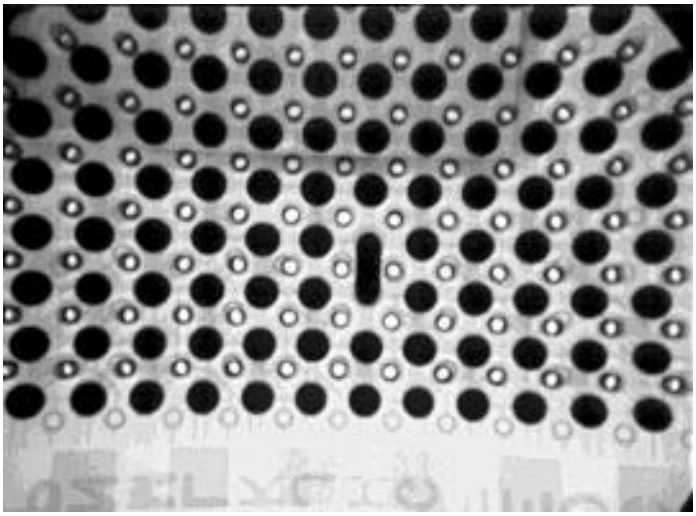

Figure 6. X-ray Micrograph of a Mounted PBGA Showing Solder Shorting

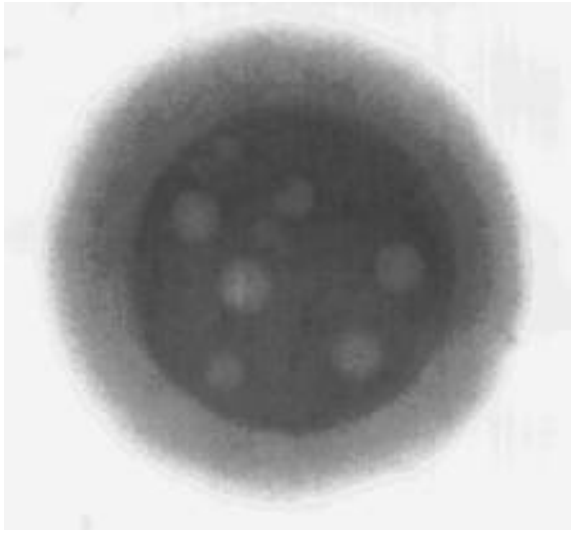

Figure 7. X-ray Micrograph of a Mounted PBGA Showing Voiding in the Solder Joints

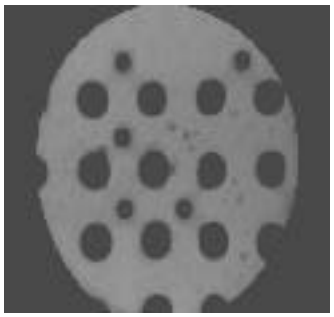

Figure 8. X-ray Micrograph of a Mounted PBGA Showing Solder Splattering/Balling

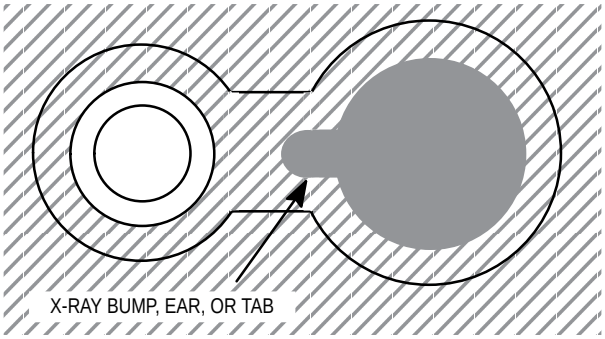

Figure 9. PBGA Pad with Bump to Facilitate X-ray Inspection

REWORK AND REPAIR

The main point that should be stressed when discussing PBGA rework is that since the assembly process gives so much better yields than high pin count, fine pitch leaded devices, that the frequency of rework is greatly reduced. Unfortunately, when one joint is defective the entire package must be replaced since there is no touchup. However, methods and equipment do exist to successfully remove and replace PBGA devices that are found to have assembly or device-related defects.

DEVICE REMOVAL

Typically, PBGA device removal involves simply heating past the solidus temperature of the solder. As opposed to the original surface mount assembly process, no special considerations (assuming the device will be scrapped) need to be taken with respect to ramp-up rates and time over solidus as long as all joints are molten upon device lifting. It may be beneficial to apply a liquid flux beneath the device prior to heating and removal. This flux will facilitate uniform heating and reduce device and board oxidation for subsequent soldering processes. Joints which were not quite molten will appear as "candy kisses" on the board and PBGA after removal. This is a good indication that the device was removed at the earliest possible time, such that the board is being subjected to a minimal amount of temperature-induced damage. If the assembled board has been exposed to out of dry-pack conditions for an extended period of time (24 to 96 or more hours depending on PBGA configuration and ambient conditions) and removal is performed, "popcorning" or die attach delamination will occur. To avoid this the entire assembly must be baked at 125°C for 12 hours. Since the saturation/bake-out curves for PBGA are quite steep, baking for a half to two-thirds of this time will go a long way in preventing popcorning as long as care is taken not to use an excessive ramp-up rate (i.e., > 3°C/min) or maximum temperature (≈ 240 – 250°C).

If other known good PBGAs (or other surface mount devices) are proximate to the device being removed, care must be taken not to overheat them and cause collateral delamination damage. Studies performed by an equipment division of Motorola who are a high volume PBGA user on devices which have body sizes of 19 mm or less indicate that neighboring devices should not exceed 185°C to prevent popcorn at any reasonable saturation level. Also, to minimize temperatures on adjacent devices the nozzle on the rework station should be maintained around 100 mils from the top of the PBGA and heating should be applied only from the top of the device. Additionally, the size of the nozzle should be less than or equal to the device molded body. As opposed to leaded devices which require perimeter heating directly to the leads, reflow of the PBGA is accomplished by heat conducting through the body of the device. Heat can be applied from the bottom also, but as stated earlier, this leads to greater spreading of the heat and an increased chance of damaging or partially reflowing neighboring devices if they are present.

EQUIPMENT

The cost of rework equipment for PBGA, as with leaded devices, varies greatly with features. Some of the features that may be useful to include in rework stations for PBGA are as follows: selectable top and/or bottom heating, selectable IR and/or forced air heating, nitrogen capability, auto-profiling capabilities, split-prism optics manual placement, automated vision placement, and a device removal head or vacuum tool. For the production rework of its smaller PBGA devices, Motorola uses a simple, inexpensive (< $4K) portable rework station made by A.P.E that provides top heating only and has no device placement capabilities. Other PBGA users are known to use the same industry-standard equipment they use for their leaded device rework made by Conceptronics, S.R.T., Air-Vac, Manix, and many others. Prices for these latter machines are ≈ $40K and up without post-removal vision placement capabilities. Of course, special PBGA-specific nozzles need to be bought or made for each of these pieces of equipment. Due to their position as a supplier of rework equipment to Motorola, A.P.E. has nozzles that correspond to most current PBGA body sizes. As PBGA popularity increases, similar nozzles and related tooling will undoubtedly be available from all rework equipment suppliers.

PRE- AND POST-REWORK BOARD CONSIDERATIONS

The principal board consideration during device removal and subsequent replacement lies in the fact that the pad may be soldermask defined and as such damage can occur if the soldermask is subjected to extreme heat and/or has poor initial adhesion to the copper pad. This situation is magnified if the board technology is soldermask over solder (SMOS) which is not recommended. If there are offset vias integral to the tear-drop shaped PBGA pad and they are not filled or tented with soldermask, the web between the usable pad and via pad will be subjected to lifting due to its potential sub 10 mil width. Also, as with reworking all SMT device types, the motherboard itself is subject to other modes of failure such as blistering, delamination and copper/PCB adhesion lifting if overheated or subjected to repeated heat cycles.

SITE PREPARATION AND DEVICE REPLACEMENT

After device removal the pads will typically have a large quantity of solder remaining (approximately half of the ball volume). This solder needs to be removed to allow device placement and facilitate self aligning of the replacement device. Removal can be performed with a solder sucker or more manually with a solder wick. The site should be fluxed prior to replacement with another PBGA device. Generally, solder paste cannot be reapplied due to the interference of a stencil and accompanying fixturing with other devices close to the removal/replacement site. Short of machine replacement with vision, the new device can be placed manually. A board design consideration to aid in this can be a silk-screen or copper pattern on the board that outlines the device body. Split prism optics that allow viewing of the PBGA bump and solder pad patterns simultaneously for alignment prior to device placement are inexpensive and have been used very successfully. The profile that is used to reflow the device should match the initial reflow profile as much as possible, although it is subject to the constraints previously discussed with regard to damaging neighboring devices.

DEVICE TEST, REBUMPING AND POSSIBLE REUSE AFTER REMOVAL

If care was taken in the removal of the device with regard to popcorning, it can ultimately be tested following reballing. If the same amount of solder remains on each pad and it is relatively hemispherical, the device can be tested as is after cleaning with a solvent. The fact that most PBGA test sockets use a pogo pin design that provides several mils (up to ≈ 20) of travel can allow testing even in the presence of smaller or even missing balls. If the bumps after removal exhibit the “candy kiss” shape, it may be necessary to flux, reflow and clean the device prior to test.

Although not recommended by Motorola, costly PBGA devices that are found to be functional can also be reworked for reuse if the process is proven reliable through a full qualification. Such rework would, of course, have to be within the allowable guidelines of the using company. Solder must first be removed from each pad as described above for the motherboard. Without a robotic bumping cell or manual bumping equipment, individual 30 mil diameter solder balls can be dipped in paste flux with tweezers (or paste flux applied to the device), placed on the removed device solder pads and then reflowed. This would definitely allow for test in any socket possibly followed by the normal reuse of the device. Undoubtedly, the time, costs and reliability of doing this need to be weighed with the original device cost to determine feasibility.

SOLDER JOINT RELIABILITY

The decreased compliance of PBGA solder joints as compared to conventional leads has raised concern about its suitability for certain applications where environments are severe (i.e., automotive), required lifetime is long (i.e., telecommunications) or device power is substantial (i.e., microprocessors). This lead compliance is important when a mounted PBGA is subjected to any thermal excursions since the joint typically absorbs the relative device/board expansion and contraction caused by thermal mismatch or temperature gradients. The materials that are used to construct the PBGA, as outlined in the earlier section on package construction, have thermal expansion coefficients that for the most part match that of the FR4/glass PCB to which they are typically mounted. The largest exception to this, for materials which are structurally significant to the package, is the silicon die. It has an expansion coefficient of 2.6 ppm/°C compared to 15 to 17 ppm/°C for other structural materials (see Table 2).

THERMAL CYCLING METHODOLOGY

Assembly-level accelerated thermal cycling is generally used to compare the performance of PBGAs relative to conventional leaded as well as other technologies. It is also used to detect any latent process defects that may be manifested in the first few cycles and to determine a wear-out (i.e., fatigue) failure distribution for the given device and environment. These test conditions are typically accelerated in cycle time as well as temperature extremes when compared to the actual application use environment. This is necessary since, by definition, an accelerated test is meant to decrease time to failure so that the failure characteristics and mechanisms may be known before the prohibitive amount of time it would take for something to fail in an actual application. Temperature extremes chosen could be the worst case expected application conditions or an expansion of that excursion to further accelerate the test. In either situation, the test will be accelerated because the cycle times chosen will probably be less than the application cycle time. A field cycle length depends on the particular application. For example, desktops personal computers are usually considered to cycle one or two times per day, while laptops cycle three to five or more cycles per day. A network server or high-end workstation may only cycle once every month on average to basically never.

The sample size in thermal cycling is generally much smaller than the ultimate population in the field. Therefore, accelerated reliability test results must be statistically analyzed and extrapolated to determine application cycles to fail a small percentage of the population. Also, these differences between cycle duration, form of excitation (i.e., internal device power versus ambient temperature swings) and temperature extremes between the accelerated test and the application field environment may need to be resolved before accurate predictions of field solder joint reliability can be made. These three differences result in a different failure distribution, namely the scale (time to 50% device failure) of that distribution, determined from accelerated testing than would be obtained by cycling to the actual application conditions. Everything involved with accounting for and resolving those differences is beyond the scope of this document, but some basic discussion to that end is included.

TESTING CONFIGURATION

Thermal cycling involves assembling PBGA devices using standard production processes to test boards that approximate the actual application board configuration in thickness, number of layers and pad geometry/layout. Some way of determining when a PBGA has failed must be used in order to gather failure data. The standard way is to use daisy-chain devices where adjacent pads are simply shorted on the PBGA substrate. Motorola has daisy-chain versions of all the PBGA designs that are currently available expressly for this purpose as well as for process studies. Traces directly connecting adjacent pads on the test board complete the chain such that there are one or more independent nets that go through all joints. An entire device can be covered with one net or several nets can be used to determine, for example, how rows fail relative to one another. Figure 10 provides an example of a routing scheme that was used on the 361 pin PBGA with 1.27 mm pitch and a 25 mm body. The rows on the device were divided into four sets: outer, middle, die perimeter, and inner.

The continuity of each net or device is measured either in-situ or every few (50 to 100 recommended) cycles to determine if it has failed. Monitoring in-situ is the preferred method and specialized equipment can be used to automate or simplify the monitoring process. Event detectors made by Anatech are especially made for monitoring solder joints, logging the data to a computer file and calculating the statistical failure parameters (discussed later) in real time. Data loggers with resistance capability may also be used.

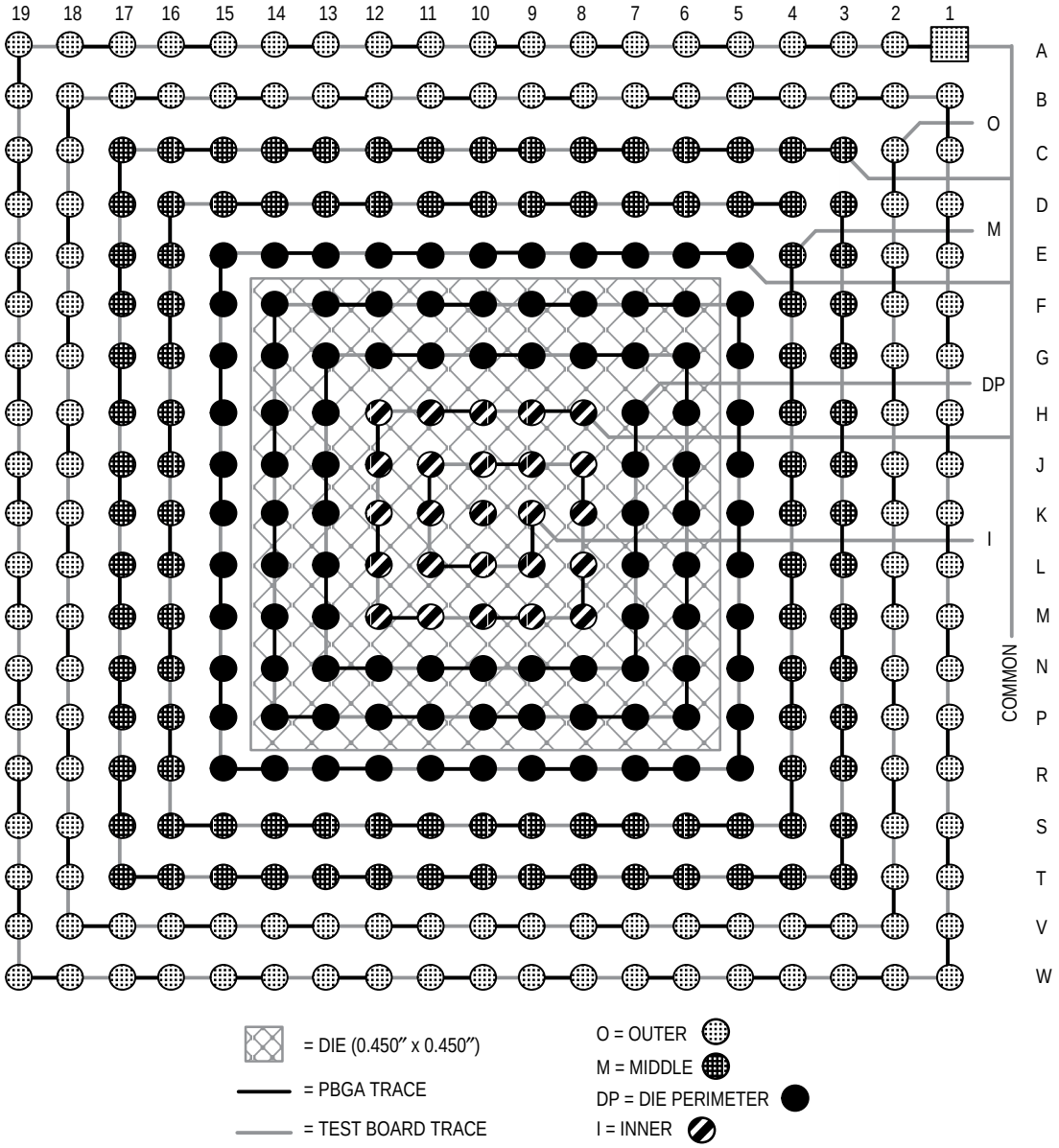

Figure 10. Example of an PBGA/Test Board Daisy-Chain Configuration to Allow Monitoring of Individual Groups of Rows (361 Pin, 19 x 19 Array, 1.27 mm Pitch, Device Bottom View)

Motorola uses two basic thermal cycle conditions. The most severe is a one hour – 40 to 125°C cycle that is mainly used to determine suitability to automotive under the hood applications. The other, more commonly used cycle is tyically 20 minutes in duration and goes from 0 to 100°C. The 20 minutes is made up of five minute ramps where possible and five minute dwell times at each temperature. The ramp time is limited by chamber heating and cooling capacity and sometimes has to be extended to allow the boards to reach the prescribed temperature. It is very important to know what temperature the boards and devices are actually experiencing as opposed to what was programmed or what the chamber air temperature is. This is accomplished through profiling the boards directly by placing thermocouples beneath several devices under which temperatures are expected to show differences. The air and board temperatures for a typical 0 to 100°C profile are shown in Figure 11. The ramp times for this profile had to be extended beyond five minutes to achieve the prescribed endpoint temperatures such that the total cycle time was 25 minutes. Examples of devices that would be expected to see the closest and furthest temperatures from the ambient air are the corner device on the board the most upstream of chamber airflow versus the middle device on the center board, respectively. To minimize these board to board thermal gradients, it is advisable to place boards parallel to the prevailing chamber air flow direction.

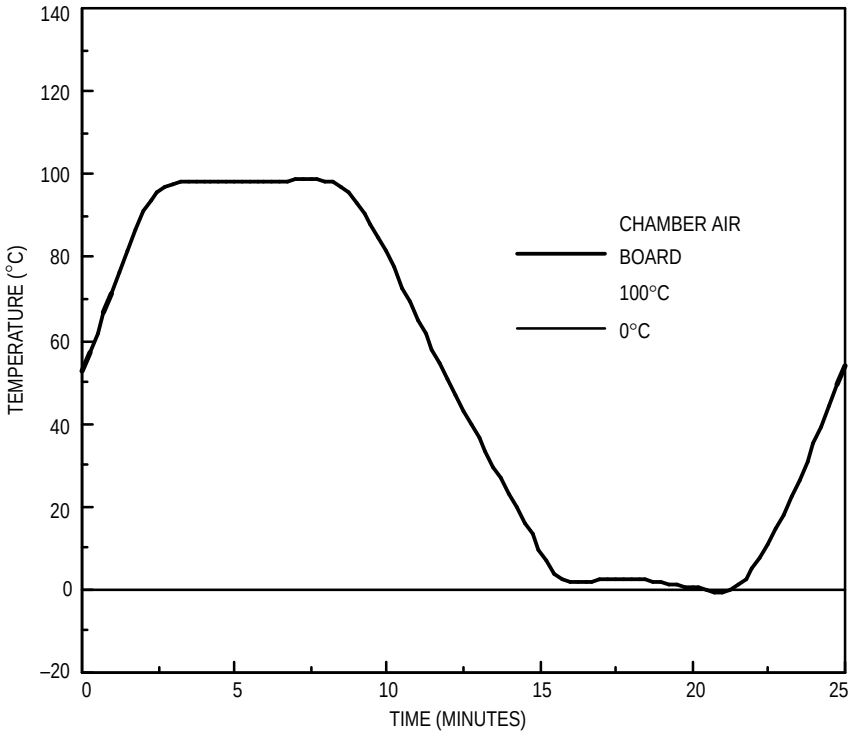

Figure 11. Typical 0 to 100°C Thermal Cycling Profile Showing the Difference Between Chamber Air Temperature and Temperature Seen by the Test Board

FAILURE DATA STATISTICAL ANALYSIS

After the thermal cycling has resulted in a substantial number of PBGA device failures (typically at least 50%, greater than 75% is preferred), the data can be fit to a statistical failure distribution. The two most commonly used for fatigue are the Weibull and the Log Normal distributions. The reliability function that describes failure in the Weibull distribution is as follows:

$$R(t) = e^{-\left(\frac{t}{\alpha}\right)^{\beta}} \quad (1)$$

In the above equation R is the fraction of devices that have survived and α and β are called the scale and shape parameters, respectively. The scale parameter, α, corresponds to the time at which 63.2% of all devices fail. Time, t, is usually expressed in cycles.

After testing is complete the data consists of a number of data pairs that is equal to the number of devices that failed. Each pair will contain the failure number and the cycles to failure for that specific device. An example of some actual data for a 225 pin PBGA that was subjected to 30 minute thermal cycles from 0 to 100°C is presented in Table 4 on the next page. In this example the sample size was 28 and cycling continued until all devices failed (100% device failure or R = 0). Larger sample sizes such as these on the order of 30 or greater are recommended. The α and β are determined by doing a best fit curve of equation (1). Statistical software packages with Weibull capability can automate the process of determining α and β. One powerful tool to do this is WeibullSmith™ (written by Fulton's Findings) and another is the software that comes with the previously mentioned Anatech event detectors. The Anatech software presents the data in terms of cycles to 50% failure as opposed to 63.2% (α). For the case of the data in Table 4, $N_{50\%}$ was determined to be 7737, α was determined to be 7958 cycles and β, which is dimensionless, was 13.0.

The data can then be plotted on Weibull axes as it is in Figure 12. Note that also plotted on this graph is the 95% lower confidence limit of the data. It is also important to note that each set of data has a correlation coefficient or a measure of its goodness of fit to the particular failure distribution. In this case, the correlation coefficient (R^2 on the graph) was an adequate 0.965.

The Log Normal distribution is similar to the Normal distribution but it operates on the logarithm of the failure data. In other words, if the distribution of the log of the cycles to failure data is normal, the data is Log Normally distributed. The reliability function for the Log Normal distribution cannot be written in closed form and is closely approximated by the following:

$$R(t) = \frac{1}{2}\left\{1 - \text{erf}\left(\frac{\ln(t) - \ln(N_{50\%})}{\sqrt{2}\sigma}\right)\right\} \quad (2)$$

Table 4. Sample Failure Data for a 225 Pin, 27 mm Body PBGA Cycled from 0 to 100°C at Two Cycles per Hour (Starting Sample Size, n = 28).

Failure Number	Cycles to Failure (t)
1	6253
2	6438
3	6536
4	6869
5	7105
6	7148
7	7195
8	7246
9	7291
10	7361
11	7405
12	7430
13	7521
14	7698
15	7720
16	7807
17	7819
18	7886
19	7887
20	7945
21	7991
22	8163
23	8197
24	8272
25	8497
26	8772
27	8874
28	9143

Once again, t is expressed in cycles and erf refers to the (Gaussian) error function. The Log Normal scale and shape parameters, $N_{50\%}$ and σ, may be calculated as mentioned previously using a best fit procedure or preferably with a statistical software package. $N_{50\%}$ is simply the mean time to failure or the time at which 50% of the sample has failed. Since 100% of the samples have failed, the Log Normal parameters can be calculated directly as follows from the cycles to failure data, with n being the sample size (Log Normal standard deviation is actually calculated on the log of the cycles to failure data):

$$N_{50\%} = \frac{\Sigma t_i}{n} \quad (3)$$

and

$$\sigma = \sqrt{\frac{\Sigma (t_i - N_{50\%})^2}{n - 1}} \quad (4)$$

Taking the same 225 pin PBGA failure data from Table 4 and fitting it to the Log Normal distribution reliability function gives an $N_{50\%}$ of 7628 cycles and a σ of 0.042. The cummulative failure 95% plot is represented in Figure 13 with the lower confidence interval shown once again. Note that for this data set the correlation coefficient (R^2) was 0.985 in the Log Normal distribution, which is better than was achieved with the Weibull distribution. Which failure distribution is used ultimately depends on how it fits the majority of the collected data as well as the availability of statistical software and familiarity with a particular distribution.

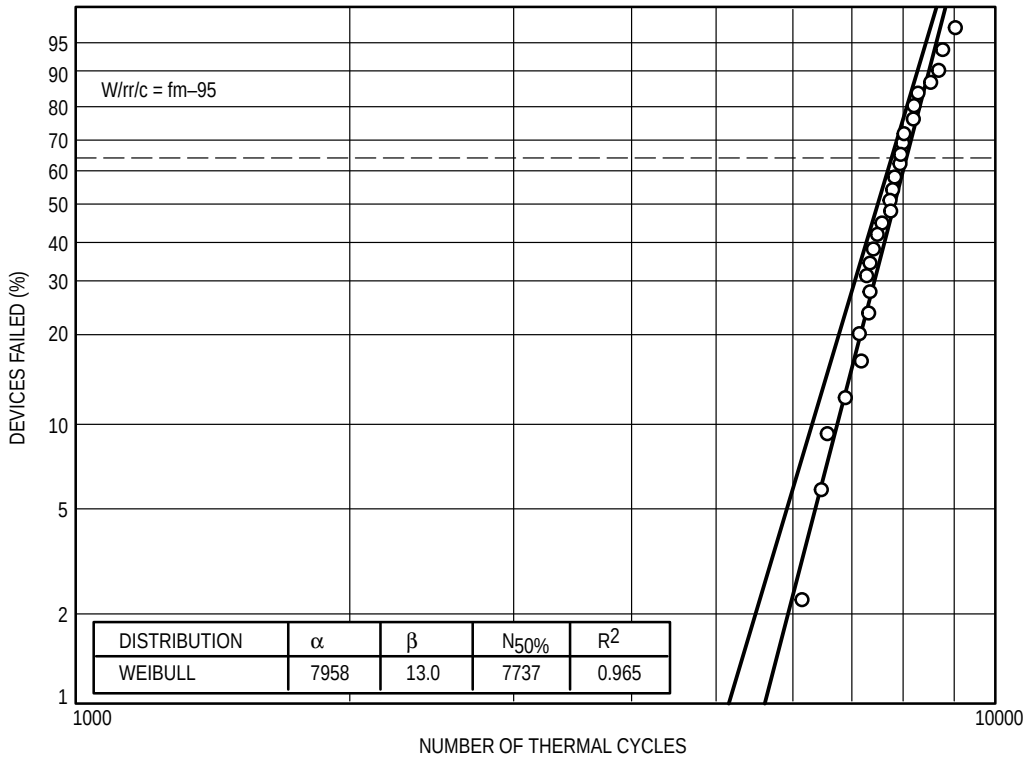

Figure 12. Weibull Failure Distribution of the Data in Table 4

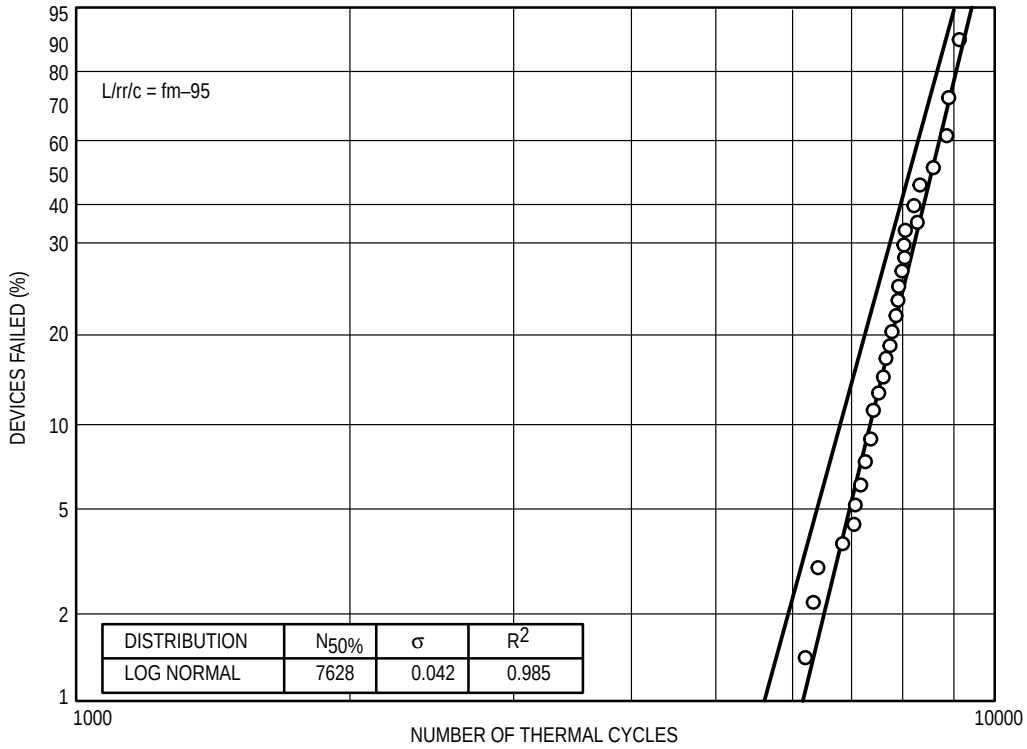

Figure 13. Log Normal Failure Distribution of the Data in Table 4

Extrapolation to Application Failure Data

As mentioned previously, PBGA accelerated reliability data and field failure data are usually different in three ways: 1) the sample size is much smaller in accelerated testing, 2) the cycle duration is greater in the actual application and 3) typical thermal excursions are usually less severe in the application. Additionally, the isothermal temperature excursions associated with thermal cycling are somewhat different than the thermal gradients found in the mounted PBGA in an actual application. The difference in the size of the population (sample size) can generally be accounted for by extrapolating data from the previously mentioned statistical distributions. Due to the highly nonlinear dependence of PBGA solder joint fatigue life on cycle time and severity, these differences generally cannot be accounted for as simply. Typically, nonlinear finite element models employing the viscoplastic temperature–dependent behavior of the solder as it undergoes creep and plastic deformation must be used. The finite element model is provided with accelerated testing and field temperature distributions for a cycle and the solder joint stress and inelastic strain or damage is determined. Crack growth and S–N correlations may then be used to determine the joint and subsequently the device life. The ratio formed by dividing the percentage of the population failing ($N_{xx\%}$) in the field (f) by the accelerated thermal cycling (ATC) testing cycles to failure is called the acceleration factor (AF):

$$AF = \frac{N_{xx\%,f}}{N_{xx\%,ATC}} \quad (5)$$

It has been proposed that a joint's, and therefore the entire package's, mean cycles to failure or $N_{50\%}$ follow a power law of the inelastic strain range seen by a joint during a thermal or application cycle (assuming inelastic strain is dominated by creep as opposed to plastic deformation):

$$N_{50\%} \propto (\Delta\varepsilon_{joint,inelastic})^n \quad (6)$$

The strain exponent (n) has been proposed by Solomon (see reference to Solomon in last section) to be approximately –2 for eutectic or near–eutectic solder. For long cycle dwell times, as would be found in typical field applications, this creep strain range is proportional to the cycle temperature range (ΔT). This temperature range raised to the strain exponent can then also be said to be proportional to the cycles to failure. For accelerated reliability testing, this is not the case unless the dwell times are sufficiently long to allow complete stress relaxation in the joint as stresses are converted to creep deformation. Substituting ΔT for $\Delta\varepsilon$ in equation (6) for both field and accelerated testing, substituting the resulting equations into equation (5) and simplifying results yields an equation of the form:

$$AF \approx \left(\frac{\Delta T_f}{\Delta T_{ATC}}\right)^{-2} \quad (7)$$

This equation has been further modified in an attempt to account for the field and ATC cyclic frequencies and maximum temperature seen during a cycle:

$$AF \approx \left(\frac{\Delta T_f}{\Delta T_{ATC}}\right)^{-1.9} \left(\frac{f_f}{f_{ATC}}\right)^{1/3} \exp\left(1414\left(\frac{1}{T_{max,f}} - \frac{1}{T_{max,ATC}}\right)\right) \quad (8)$$

Where: f, ATC = Subscripts to indicate field and accelerated thermal cycling testing.

$N_{xx\%}$ = Percentage of devices failed.

ΔT = Difference in minimum and maximum cyclic extremes (°C).

f = Cyclic frequency (Note: For purposes of the above equation, f_f minimum is 6 cycles per day).

T_{max} = Maximum during a cycle temperature (°K).

Once again, such an equation should be used as a very rough first–order estimate and could give very erroneous results, but it may be used for a lack of any other more in–depth analysis (such as nonlinear finite element modeling). It is also prudent to obtain an actual acceleration factor from two different testing conditions to verify the validity of equation 8 before its use in predicting field cycles to failure.

After the acceleration factor, scale parameter and shape parameter have been determined, test data may be extrapolated to determine cycles to failure for a much larger sample size such as a population in the field. The acceleration factor is multiplied by the percentage failed in accelerated thermal cycling to determine the percentage failed in the field as follows:

$$N_{xx\%,f} = AF \bullet N_{xx\%,ATC} \quad (9)$$

Then the time for any percentage to fail in the field can simply be calculated by substituting the desired reliability (i.e., fraction failed), the shape parameter and the field scale parameter and solving for time (in cycles) in either equations (1) or (2) above. It also has to be assumed that the field shape parameter (β or σ) is the same as that calculated from testing. This then assumes that the failure mode is the same in both the field and during accelerated testing since the shape parameter is also an indicator of failure mode. For the Weibull distribution, solving equation (1) for time yields:

$$t = \alpha \bullet \{-1n\,[R(t)]\}^{(1/\beta)} \quad (10)$$

It must be determined to what reliability cycles to failure are desired. It is commonly desirable to know the time at which 1,000 devices per million (ppm) would be predicted to fail. This 1,000 ppm corresponds to an R of 0.999 (R = 1 – 1,000/1,000,000=1 – fraction failed). Substituting this R as well as a previously calculated value of α ($N_{63.2\%}$) and known β into equation (10) yields a time to fail 1,000 ppm or $N_{0.1\%}$ of 4685 cycles. Since the Lognormal equation (2) cannot readily be solved for time due to its complexity, an iterative process (with the aid of a spreadsheet that has the erf function) can be performed to determine the $N_{0.1\%}$. Alternately, statistical software with Lognormal capabilities may be used. For this example it was determined to be 5659 cycles. This is slightly higher than what was predicted using the Weibull distribution. This is usually the case, as the Weibull distribution is a more conservative predictor than the Lognormal. However, the Lognormal traditionally results in a better correlation coefficient. The distribution that is used should be whatever the user is most comfortable and has the most experience or history using. Predictions to any given reliability can likewise be made from the two distributions. To illustrate this and to further compare the Weibull and Lognormal distributions, Table 5 shows a range of reliabilities calculated from using the data in Table 4.

It should be noted that to extrapolate the most conservative cycles to failure values for small percentages of a total population, data to a desired confidence interval should be used. In the two reliability plots above (Figures 12 and 13) this would mean using the lines forming the 90% confidence interval (or whatever confidence level was desired) as opposed the scale and shape parameters determined from the best fit of the data. It is only practical to consider the lower confidence limit since using the upper limit of the expected cycles to failure is not useful or prudent for field failure prediction. Table 6 compares the predicted cycles to failure from the best fit line versus those predicted using the upper and lower 95% confidence limits.

PBGA Thermal Cycling Data

Motorola has thermal cycled several configurations of 72, 119, 225, and 361 pin PBGAs while testing of other configurations is ongoing. Additionally, several other companies have thermal cycling testing either underway or completed. Two of those companies are AT&T and Compaq and their published data, along with a sampling of Motorola data are presented in Table 7. Also listed are Motorola data on two leaded devices, the 68 PLCC and the 208 PQFP, both with copper leadframes. The Motorola PBGA data shown shaded in Table 7 represents data that was used as example data for thermal cycling statistics in the previous section.

Table 5. 225 Pin PBGA Reliability Predictions Using the Weibull and Log Normal Distributions (0 to 100°C Thermal Cycling, 20 Minute Cycle)

Reliability (R)	Percentage Failed (%)	Devices Failed Per Million	Predicted Cycles to Failure Using:	
			Weibull	Log Normal
0.999999	0.0001	1	2758	4794
0.99999	0.001	10	3291	5035
0.9999	0.01	100	3926	5317
0.999	0.1	1000	4685	5659
0.99	1.0	10,000	5592	6098
0.9	10.0	100,000	6696	6739
0.84	16.0	160,000	6960	6925
0.5	50.0	500,000	7737	7628
0.368	63.2	632,121	7958	7878

Table 6. Reliability Predictions Using the Lower 95% Confidence Limits for the Weibull and Lognormal Distributions

	Predicted $N_{0.1\%}$ (in Cycles) Using:	
	Weibull	Log Normal
From Best Fit Line	4685	5659
95% Lower Confidence Limit	4121	5239

Table 7. PBGA Accelerated Thermal Cycling Data from Motorola and Others(with Comparisons to PQFP/PLCC)

Company	Device (Die in mils)	Cycle (°C)	$N_{0.1\%}$	$N_{1\%}$	$N_{50\%}$	α ($N_{63\%}$)	β	Source
Motorola	72 PBGA (270x270)	– 40 to 125, 1cph	1058	1363	2171	2260	9.1	Internal
Motorola	72 PBGA (270x270)	0 to 100, 3cph	3013	4034	6895	7222	7.9	Internal
Motorola	119 PBGA (280x437)	0 to 100, 2cph	4459	5848	9683	10113	8.4	Internal
Motorola	225 PBGA (400x400)	0 to 100, 2cph	4685	5592	7737	7958	13.0	Internal
Motorola	361 PBGA (450x450)	0 to 100, 2cph	6319	7804	11495	11886	10.9	Internal
Motorola	68 **PLCC**, Cu Leadframe	– 40 to 125, 1cph	904	1818	6561	7332	3.3	Internal
Motorola	208 **PQFP**, Cu Leadframe	– 40 to 125, 1cph	639	1553	7912	9111	2.6	Internal
AT&T	169 PBGA (364x359)	0 to 100, 2cph	2103	2741	4459	4651	8.7	Semi/HDP-10/93
AT&T	225 PBGA (389x398)	0 to 100, 2cph	1412	1993	3749	3960	6.7	Semi/HDP-10/93
Compaq	72 PBGA (270x270)	– 25 to 100, 2cph	1734	2194	3379	3508	9.8	1993 IEPS
Compaq	165 PBGA (437x437)	– 25 to 100, 2cph	1010	1309	2106	2195	8.9	1993 IEPS
Compaq	225 PBGA (389x398)	– 25 to 100, 2cph	1252	1664	2807	2937	8.1	1993 IEPS

Comparing the cycles to 50% failure for the PBGA and leaded devices reveals that the PQFP and PLCC tend to last longer. For example, $N_{50\%}$ for the 68 PLCC is a factor of three greater (6561 versus 2171 cycles) than the 72 PBGA for identical cycling conditions. But, it can be seen in Table 7 that the β's associated with leaded device data are significantly lower, on average, than those of the PBGA. This greater spread in the leaded device data can be attributed to a greater variation in the factors that influence solder joint reliability such as solder volume and device coplanarity. This β disparity means that there is a greater spread in the leaded data and when subsequent extrapolations are made down to $N_{0.1\%}$ or lower, they tend to become comparable to the same estimates for PBGA. Extrapolating $N_{0.1\%}$ for the 72 PBGA and 68 PLCC mentioned above, yields 1058 and 904 cycles, respectively. The same thing can be done when comparing the 225 PBGA to the 208 PQFP although the thermal cycle on the leaded device was the more severe – 40 to 125°C. The 208 PQFP had a higher α and $N_{50\%}$, but when $N_{0.1\%}$'s are compared there is a much different situation (4685 cycles PBGA versus 639 cycles PQFP).

Another observation from Motorola testing is that rows under and proximate to the die perimeter tend to fail first. This can be seen in Figure 14 which compares the outer, die perimeter, middle, and inner rows of the standard 361 pin PBGA. This gets back to the previously mentioned mismatch between silicon and the other PBGA and FR4 PCB materials. To further prove this point, tests on 72 pin packages without die went for many more cycles without failure than identical packages with die. Another conclusion drawn from Motorola testing is that there is a relative cycle basis acceleration factor of about 3.5 between 0 to 100°C and – 40 to 125°C PBGA testing. This actually results in no relative acceleration on a time basis since the more severe cycle is approximately three times longer than the 0 to 100°C cycle. Also observed from the testing was that underfill (although it causes the devices to be unreworkable) can give up to a 4X increase in cycles to failure and that increased device standoff (obtained through using larger diameter solder balls) improves the fatigue life as would be expected.

Failure Analysis

Analysis of devices that have failed in accelerated thermal cycling or in an application can provide extremely useful information with regard to determining the failure characteristics and mode. Generally, the failure analysis of PBGA devices consists of resistance probing to locate specific failed joints when possible, cross-sectioning and also die penetrant analysis of fractures. Probing of individual joints (actually joint pairs) usually only pertains to daisy-chain devices on test boards that have vias integral to each solder pad which drop down to the bottomside of the board and can be probed. Knowing the schematic of the daisy-chain net, specific via pairs can be probed until a failing pair with atypical or infinite resistance is found.

Care must be taken when preparing cross-sections of PBGAs with solder joint failures. Vibrations and flexure caused by the cutting of a failed device out of a test board, if not performed properly, can further propagate or initiate fractures. High speed diamond blades, abrasive wheels or routers are recommended over band saws. Once the device is removed, setting of the potting compound should optimally take place in a vacuum. Slower curing potting epoxies are also usually better than the quick setting variety to ensure that the PBGA is completely underfilled. After grinding, polishing and etching to reveal the solder structure, fractures

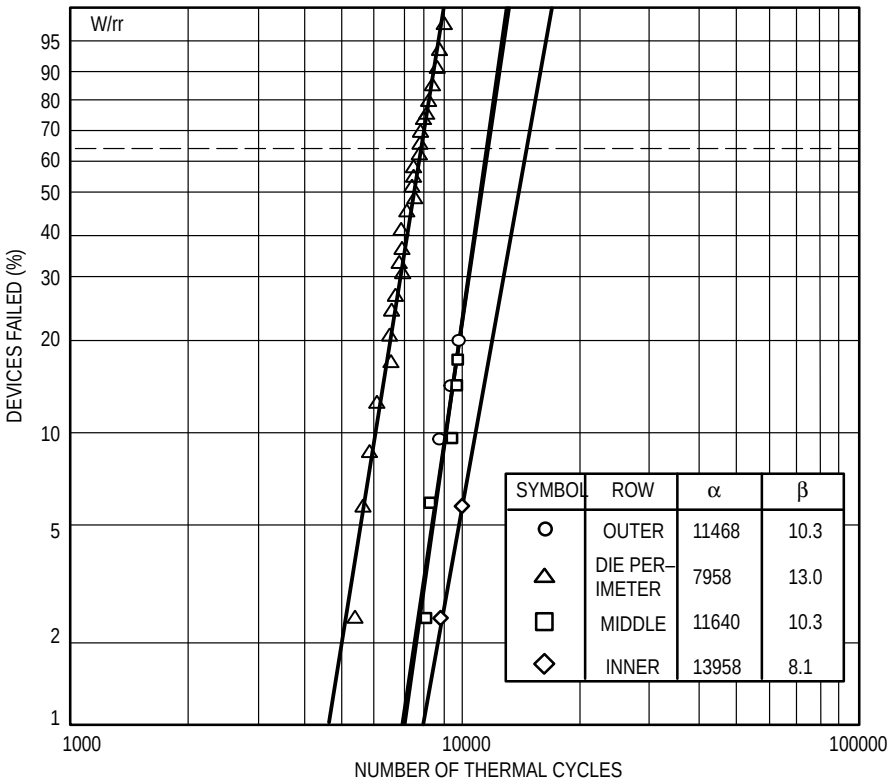

Figure 14. Weibull Failure Distribution by Device Row for a 361 Pin PBGA Cycled from 0 to 100°C at Two Cycles per Hour

can be readily observed. It should be noted that fracture length measurements taken from perpendicular PBGA cross-sections can be erroneous, depending on the row being sectioned, due to the fact that fractures generally propagate in a direction radially from the device center.

A very useful technique in analyzing devices with a multitude of fractured joints is dye penetrant analysis. Dye penetrant analysis can be used to visualize an overall distribution of fractures on all joints. For this procedure to work the best, the mounted device should be cleaned with a solvent prior to the application of a dye penetrant. This cleaning removes any flux residues, soldermask and other particles which are mobile during thermal cycling and may inhibit the flow of the dye into the fracture. There are many dyes available for the specific purpose of penetrating fractures (such as Ardrox Tracer-Tech), however, a machinist's layout dye made by ITW and called Dykem (Steel Red is typically the most visible) has shown excellent results at Motorola and elsewhere. After cleaning, a dropper is used to repeatedly flush the dye underneath the mounted device. The excess dye is then allowed to drain and the remainder is dried. This drying is accelerated by baking at 100°C for 10 to 30 minutes depending on the amount of dye under and around the device. Following removal from the bake oven and cooling, the PBGA is mechanically removed. It can be pried off with a screwdriver or similar, which may damage joints on the outer one or two rows, or the board repeatedly flexed until the device "pops" off. After removal, the board and device can be readily inspected. Fracture surfaces which are dyed were obviously present prior to device removal and presumably caused by the accelerated testing. An example with a fracture approximately one quarter of the way through the joint is presented in Figure 15.

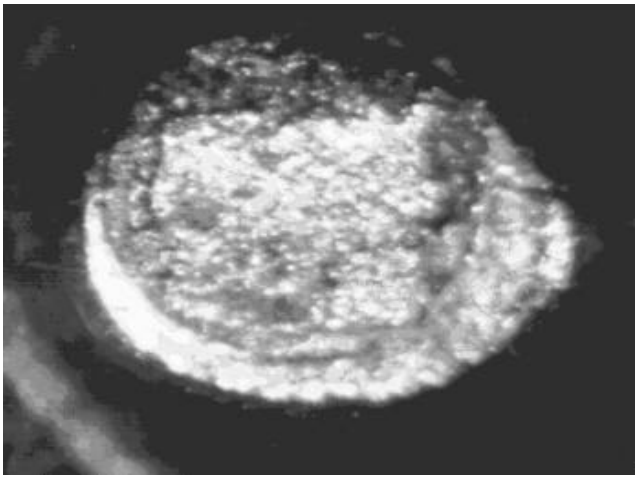

Figure 15. Micrograph of a Solder Joint Partial Fracture Surface Following Application of Dye Penetrant and Removal of a Thermal Cycled PBGA (Magnification of ≈ 50X)

MOISTURE AND POPCORNING

As with all plastic surface mount packages, the PBGA is currently susceptible to moisture induced delamination or popcorning if it is heated to reflow temperatures with excessive moisture content. The moisture weight percentage at which damage can occur is typically 0.15%. The PBGA is currently specified to meet Level 5 of the JEDEC classifications for moisture sensitivity in Test Method A112 (JESD22–A112). Level 5 in this test method, states that the PBGA will not exhibit delamination after exposure to 30°C/60%RH for 30 hours. The accompanying user handling requirements are a 24 hour out or drypack life. Any exposure over this 24 hours will require baking at 125°C for 24 hours. It is recommended, where possible, that this bake be performed in an inert atmosphere such as nitrogen to minimize potential solder ball oxidation.

The mode of moisture-induced failure in the PBGA package is delamination of the die attach from the die flag. This delamination, caused by the vaporization of the trapped moisture, is clearly visible in the form of a bubble in the BT substrate immediately under the die location. If the moisture content is high enough this delamination occurs violently (i.e., popcorning) and the delamination will propagate along the mold compound/BT interface until it is visible around the perimeter of the package. When this occurs, it is likely that an accompanying shorting of solder balls will occur in the area under the die. For this reason, it is advised to bake and dry pack even mechanical samples or daisy-chain devices prior to process assembly experiments.

RELIABILITY STRESS TESTS

The following summary briefly describes the various reliability tests included in the packaging reliability program. This program includes the PBGA.

SMT Preconditioning Stress

The purpose of this test is to simulate the shipping, storage, and solder attach steps involved in mounting and reworking a surface mount device. The preconditioning flow begins with ten temperature cycles at –65 to 150°C, dehydration bake at 125°C for 24 hours and is followed by a moisture soak. The moisture soak may involve simulating a worst case “no dry pack” condition in an 85°C/85% RH environment, a worst case dry pack condition of 85°C/60% RH, or a typical manufacturing environment condition of 30°C/60% RH. The duration of the moisture condition will vary depending on the moisture level tested. Moisture exposure is followed by two passes of infrared reflow (230°C) for 20 seconds per pass. Infrared reflow equipment is capable of heating the top side package body to 230°C with a ramp rate of 2–10°C per second.

Temperature Cycle

This test accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. This test is typically performed to minimum and maximum temperatures of –65 to 150°C for a duration of 500 or 1000 cycles. During temperature cycle testing, devices are inserted into a cycling system and held at a cold dwell system for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minutes. the system employs a circulating air environment to assure rapid stabilization at the specified temperature.

Thermal Shock

The objective of this test is the same as that for temperature cycle testing: to emphasize differences in expansion coefficients for components of the packaging system. However, thermal shock provides additional stress because the device is exposed to a sudden change in temperature due to the transfer time of ten seconds maximum as well as the increased thermal conductivity of a liquid ambient. This test is typically performed to a minimum and maximum temperatures of –65 to 150°C for a duration 500 or 1000 cycles. Devices are placed in a fluorocarbon bath and cooled to minimum specified temperature. After being held in the cold chamber for five minutes, the devices are transferred to an adjacent chamber filled with fluorocarbon at the maximum specified temperature for an equivalent time. Two five minute dwells plus two ten second transitions constitute one cycle.

Temperature Humidity Bias (THB)

This is an environmental test performed at a temperature of 85°C. The test is designed to measure the moisture resistance of plastic encapsulated circuits. A nominal static bias is applied to the device to create the electrolytic cells necessary to accelerate corrosion of the metallization. Typical stress duration is 1008 hours.

Autoclave

Autoclave is an environmental test that measures devices resistance to moisture penetration and the resultant effects of galvanic corrosion. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psig. Corrosion of the die is the expected failure mechanism. Autoclave is a highly accelerated and destructive test. Typical test duration is 96 hours.

Results from a qualification of an 86 pin PBGA are included in Appendix D.

RELATED TECHNICAL ARTICLES AND PAPERS

This section provides only a partial listing of articles that have appeared in trade journals and have been published in conference proceedings that discuss issues related to PBGA. All articles are listed alphabetically by principal author/editor last name. Articles for which there is no copyright may be available informally through Motorola.

R. Boyd-Merritt, “Moto Fields New Package Technology”, *Electronic Engineering Times*, March 1, 1993, p. 70.

T. Costlow, “Moto Pact Big for BGAs?”, *Electronic Engineering Times*, August 2, 1993, p. 16.

R. Darveaux and K. Banjeri, “Fatigue Analysis of Flip Chip Assemblies Using Thermal Stress Simulations and a Coffin-Manson Relation”, Proceedings of ECTC, 1991.

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R. Darveaux, “Crack Initiation and Growth in Surface Mount Solder Joints,” Proceedings ISHM 25th International Symposium on Microelectronics, Dallas, TX, 1993.

M. Donlin, “Packaging Innovations Help Engineers Break Free from Design Constraints”, *Computer Design*, June 1993, pp. 65 – 68.

B. Freyman and R. Pennisi, “Overmolded Plastic Pad Array Carriers (OMPAC): A Low Cost, High Interconnect Density IC Packaging Solution for Consumer and Industrial Electronics”, Proceedings of the Technical Conference, 1991 ECTC, pp. 176 – 182.

A. Fukuda, Feature Article on BGAs (in Japanese), *Nikkei Electronics*, February 14, 1994, pp. 59 – 73.

D. Hattas, “BGAs Face Production Testing”, *Advanced Packaging*, Summer 1993, pp. 44 – 46.

J. Houghten, “New Package Takes on QFP’s”, *Advanced Packaging*, Winter 1993, pp. 38 – 39.

R. Johnson, A. Mawer et al., “A Feasibility Study of Ball Grid Array Packaging”, NEPCON East Proceedings, 1993, pp. 413 – 425.

R. Johnson and D. Cawthon, “Thermal Characterization of 140 and 225 Pin Ball Grid Array Packages”, NEPCON East Proceedings, 1993.

J. Lau et al., “No Clean Mass Reflow of Large Over Molded Plastic Pad Array Carriers (OMPAC)”, 1993 IEEE/CHMT International Electronics Manufacturing Technology Symposium Proceedings, pp. 63 – 75.

D. Maliniak, “BGAs Make Transition to Memory Packages”, *Electronic Design*, October 14, 1993, pp. 34 – 35.

H. Markstein, “Pad Array Improves Density”, *Electronic Packaging & Production*, May 1992, pp. 25 – 26.

F. Martin, “C-5 Solder Sphere Robotic Placement Cell for Overmolded Pad Array Carrier”, 1993 International Electronics Packaging (IEPS) Conference Proceedings, pp. 740 – 748.

A. Mawer, R. Darveaux and M. Petrucci, “Calculation of Thermal Cycling and Application Fatigue Life of the Plastic Ball Grid Array (BGA) Package”, 1993 International Electronics Packaging (IEPS) Conference, 1993, pp. 718 – 730.

B. Miles and B. Freyman, “The Elimination of the Popcorn Phenomenon in Overmolded Plastic Pad Array Carriers (OMPAC)”, 1992 International Electronics Packaging (IEPS) Conference Proceedings, pp. 605 – 614.

K. O’Brien, “Will BGA Live Up to Its Billing”, *Surface Mount Technology*, August 1993, p. 40.

B. Nagaraj and M. Mahalingam, “OMPAC Package — Creep Analyses of C5 Solder Pads Using FEM Simulation,” APDC Technical Report 15-92, 1992.

J. Shimizu, “Plastic Ball Grid Array Coplanarity”, Proceedings of the 1993 Surface Mount International Conference, pp. 86 – 90.

H. Solomon, “Strain-Life Behavior in 60/40 Solder”, GE Report #88CRD261, 1988.

C. Trigas, “The OMPAC Package — Assembly to Printed Circuit Board”, Proceedings of the 1994 EuPAC Conference, Feb 1 – 3, 1994, Essen, Germany.

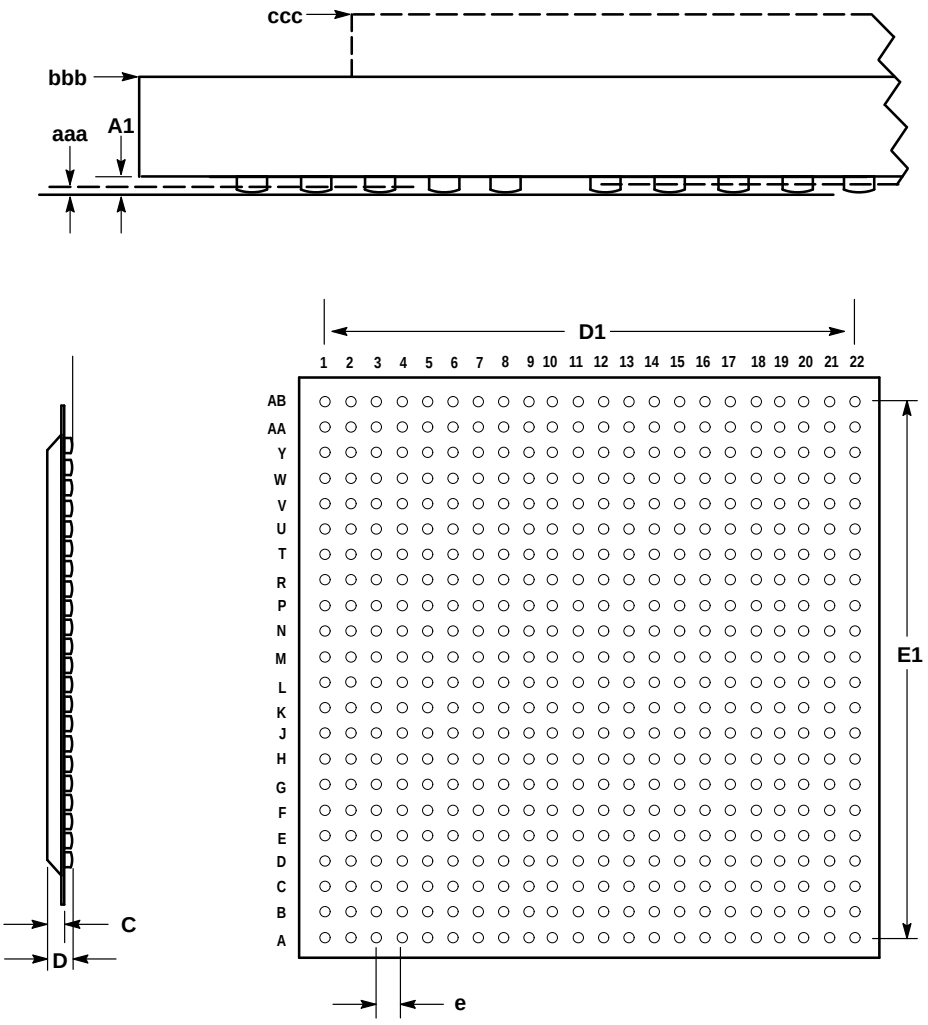
J. Tuck, “BGAs: A Trend in the Making”, *Circuits Assembly*, December 1993, pp. 20 – 21.

J. Tuck, “BGAs: The Next Chapter”, *Circuits Assembly*, August 1993, pp. 24 – 27.

J. Vardaman, “Ball Grid Array Packaging”, TechSearch International, Inc. Consulting Report, January, 1993.

W. Yip and C. Tsai, “Electrical Performance of an Overmolded Pad Array Carrier (OMPAC), 1993 International Electronics Packaging (IEPS) Conference Proceedings, pp. 731 – 739.

APPENDIX A
JEDEC PLASTIC BALL GRID ARRAY FAMILY REGISTRATION



Reference Composite of 1.00, 1.27 and 1.50 Pitch Matrices

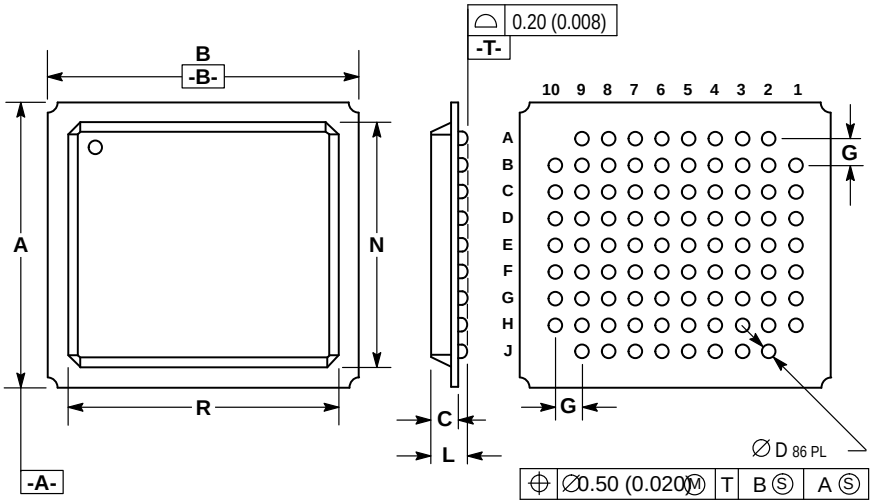
D / E	e = 1.00			e = 1.27			e = 1.50		
	M	N		M	N		M	N	
		Full Matrix	Stagger Matrix		Full Matrix	Stagger Matrix		Full Matrix	Stagger Matrix
7.00	6	36	—	5	25	—	4	16	—
9.00	8	64	—	7	49	—	6	36	—
11.00	10	100	—	8	64	—	7	49	—
13.00	12	144	—	10	100	—	8	64	—
15.00	14	196	—	11	121	—	10	100	—
17.00	16	256	—	13	169	—	11	121	—
19.00	18	324	—	15	225	—	12	144	—
21.00	20	400	—	16	256	—	14	196	—
23.00	22	484	242	18	324	—	15	225	—
25.00	24	576	288	19	361	—	16	256	—
27.00	26	676	338	21	441	221	18	324	—
29.00	28	784	392	22	484	242	19	361	—
31.00	30	900	450	24	576	288	20	400	—
33.00	32	1024	512	26	676	338	22	484	242
35.00	34	1156	578	27	729	365	23	529	265
37.50	37	1369	685	29	841	421	25	625	313
40.00	39	1521	761	31	961	481	26	676	338
42.50	42	1764	882	33	1089	545	28	784	392
45.00	44	1936	968	35	1225	613	30	900	450
47.50	47	2209	1105	37	1369	685	31	961	481
50.00	49	2401	1201	39	1521	761	33	1089	545

Solder Ball Dimensions and Package Coplanarity

Dimension	e = 1.00			e = 1.27			e = 1.50		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
aaa	—	—	.15	—	—	.15	—	—	.15
bbb	—	—	.25	—	—	.25	—	—	.25
ccc	—	—	.35	—	—	.35	—	—	.35
b	.50	.60	.70	.60	.75	.90	.60	.75	.90
A1	.40	.50	.60	.50	.60	.70	.50	.60	.70

APPENDIX B
PACKAGE MECHANICAL OUTLINES FOR THE 86, 119, 169, 225, and 357 PIN PBGA

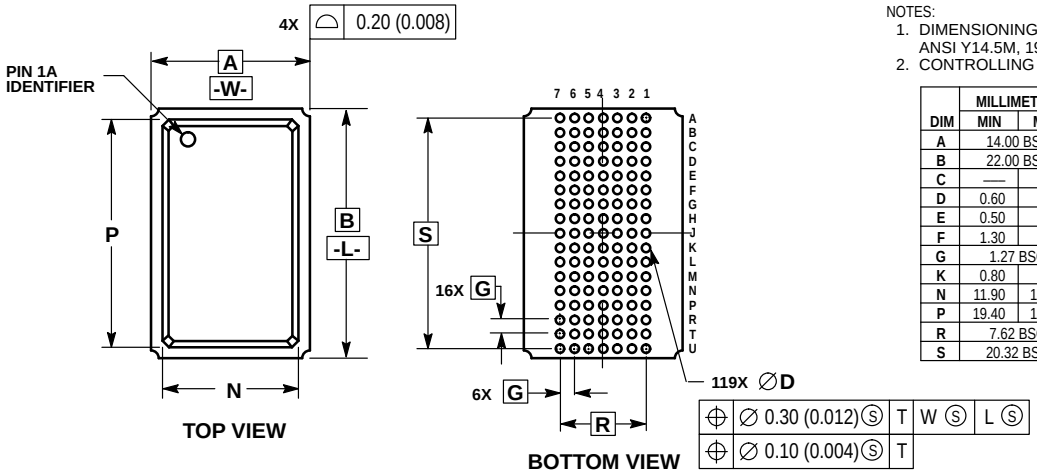
86 PIN PBGA
CASE 896A-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

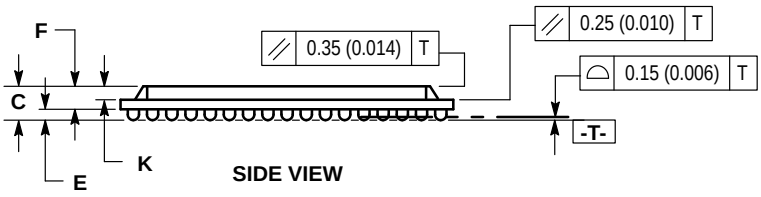
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	16.16	16.36	0.637	0.644
B	17.68	17.88	0.697	0.703
C	1.33	1.73	0.053	0.068
D	0.69	0.81	0.028	0.031
G	1.524 BSC		0.060 BSC	
L	1.84	2.44	0.073	0.096
N	13.80	14.20	0.544	0.559
R	15.29	15.69	0.602	0.617

119 PIN PBGA
CASE 999-01

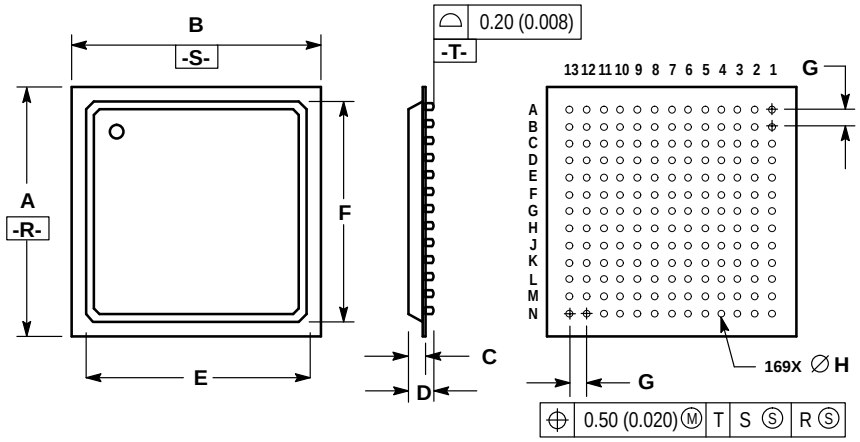


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.00 BSC		0.551 BSC	
B	22.00 BSC		0.866 BSC	
C	—	2.40	—	0.094
D	0.60	0.90	0.024	0.035
E	0.50	0.70	0.020	0.028
F	1.30	1.70	0.051	0.067
G	1.27 BSC		0.050 BSC	
K	0.80	1.00	0.031	0.039
N	11.90	12.10	0.469	0.476
P	19.40	19.60	0.764	0.772
R	7.62 BSC		0.300 BSC	
S	20.32 BSC		0.800 BSC	



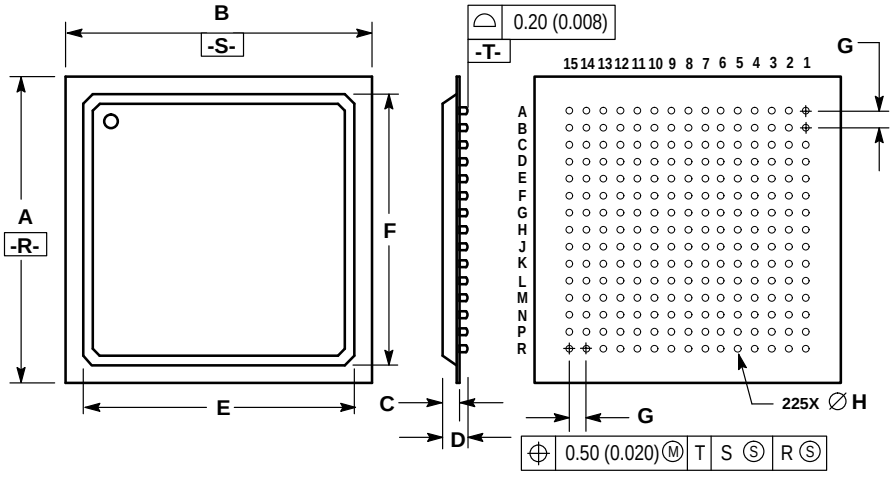
169 PIN PBGA
CASE 938-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	21.90	22.10	0.8622	0.8700
B	21.90	22.10	0.8622	0.8700
C	1.33	1.73	0.0523	0.0681
D	1.83	2.43	0.0720	0.0956
E	19.30	19.70	0.7598	0.7755
F	19.30	19.70	0.7598	0.7755
G	1.50 BSC		0.0590 BSC	
H	0.690	0.810	0.0271	0.0318

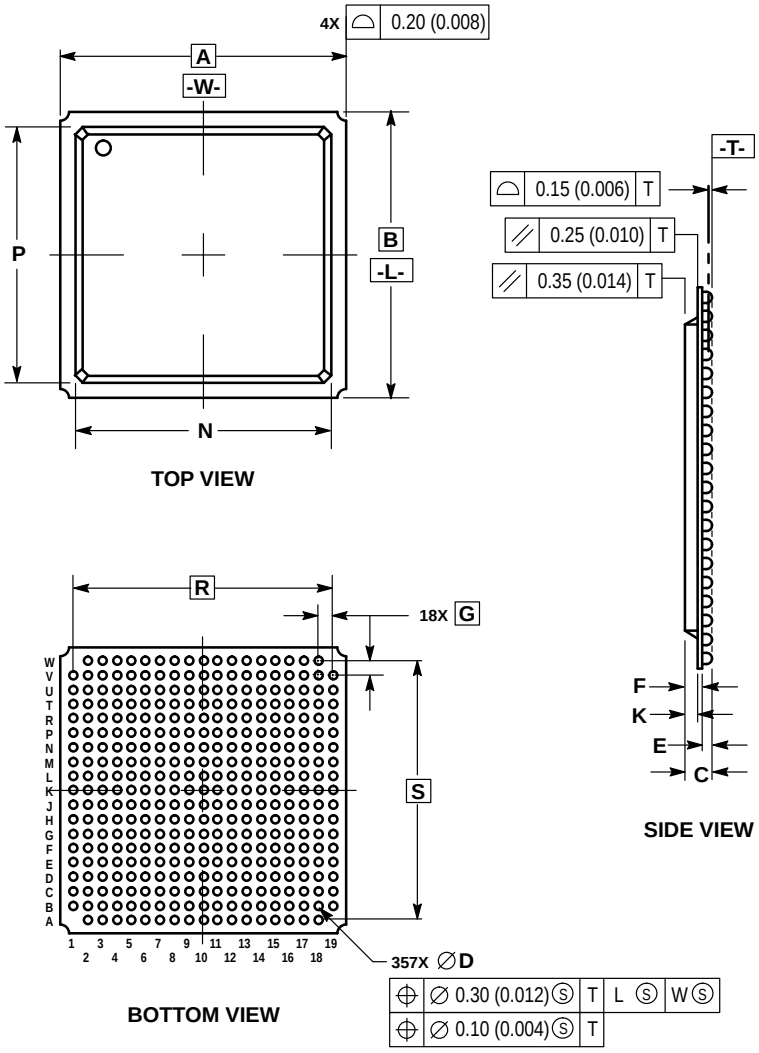
225 PIN PBGA
CASE 938A-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	26.90	27.10	1.0590	1.0669
B	26.90	27.10	1.0590	1.0669
C	1.33	1.73	0.0523	0.0681
D	1.83	2.43	0.0720	0.0956
E	23.80	24.20	0.9370	0.9527
F	23.80	24.20	0.9370	0.9527
G	1.50 BSC		0.0590 BSC	
H	0.690	0.810	0.0271	0.0318

357 PIN PBGA
CASE 1103-01



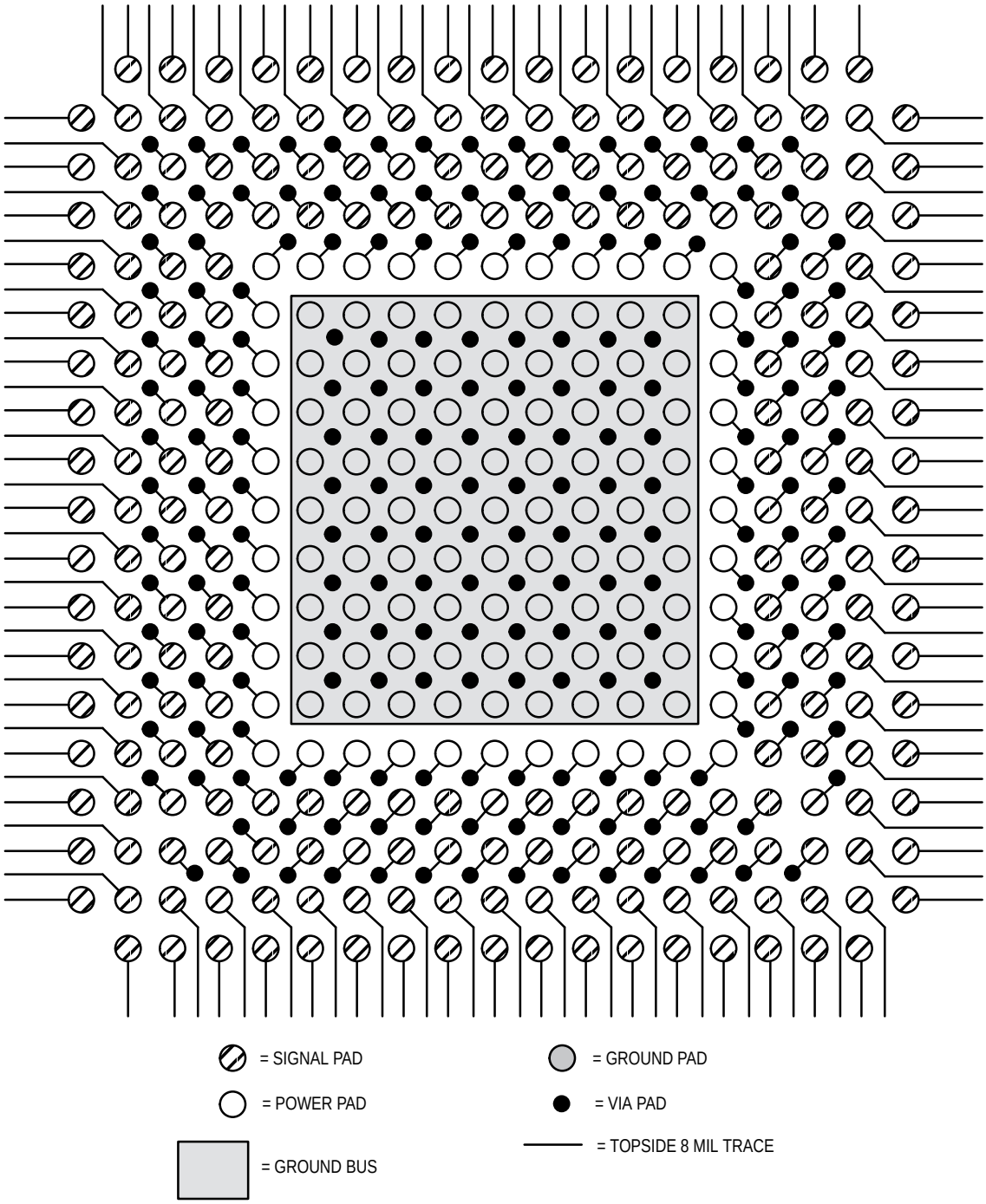
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.00 BSC		0.984 BSC	
B	25.00 BSC		0.984 BSC	
C	—	2.05	—	0.081
D	0.60	0.90	0.024	0.035
E	0.50	0.70	0.020	0.028
F	0.95	1.35	0.037	0.053
G	1.27 BSC		0.50 BSC	
K	0.70	0.90	0.028	0.035
N	22.40	22.60	0.882	0.890
P	22.40	22.60	0.882	0.890
R	22.86 BSC		0.900 BSC	
S	22.86 BSC		0.900 BSC	

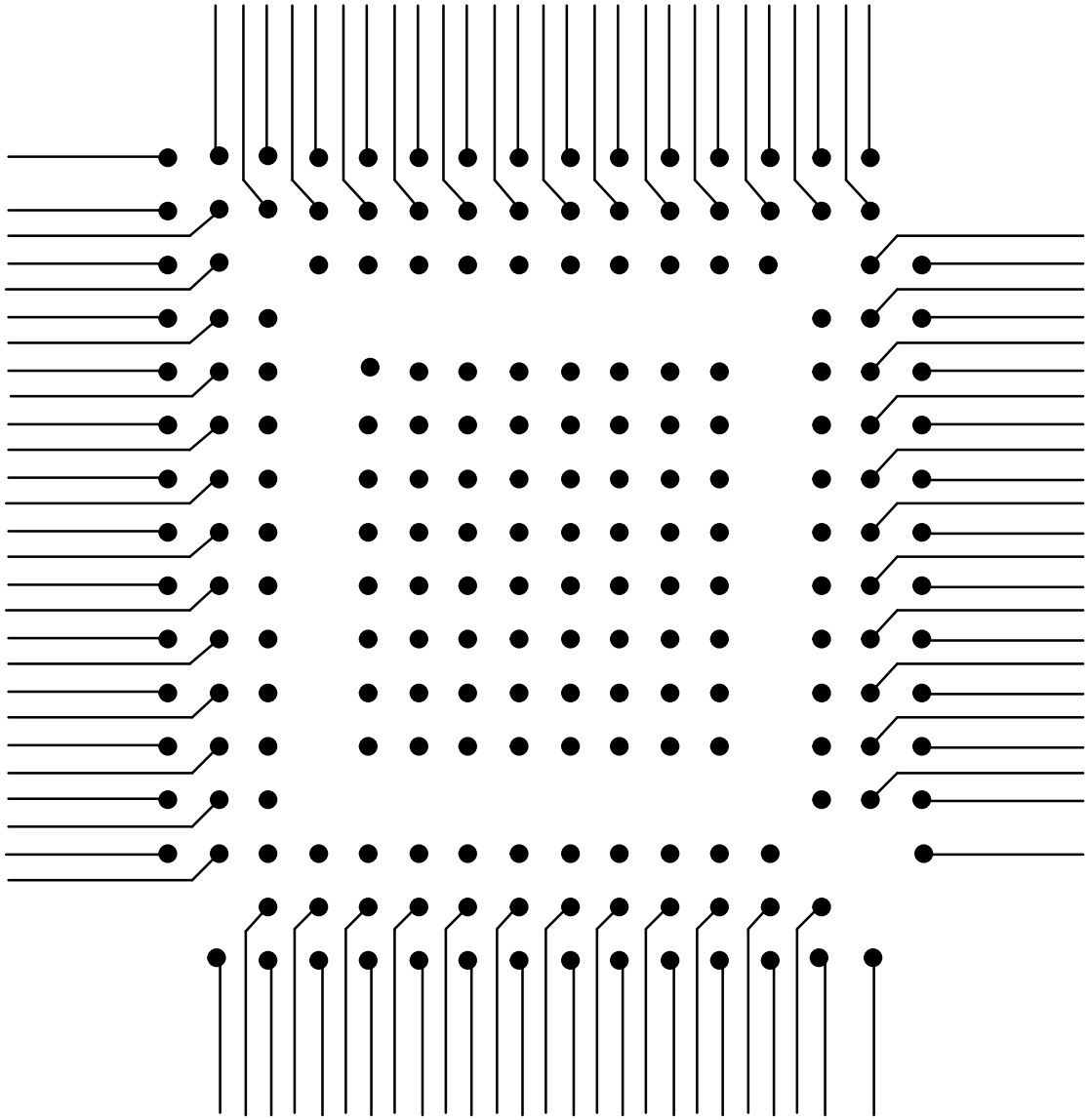
APPENDIX C

Example of escape routing for a 19x19 array, 1.27 mm pitch 357 pin PBGA with 23 mil diameter NSMD solder pads on a board with two signal, one power, and one ground plane.

TOP LAYER METAL



BOTTOM LAYER METAL



● = 25 MIL VIA PAD

—— = BOTTOMSIDE 8 MIL TRACE

APPENDIX D

86 PIN PBGA PACKAGE QUALIFICATION SUMMARY SHEET

SOURCE DEVICE:	**MCM62C416ZP21**	TECHNOLOGY:	**0.8 µ CMOS**	FABRICATION:	**MOS8**
SOURCE DEVICE:	**MCM56824ZP25**	TECHNOLOGY:	**0.8 µ CMOS**	FABRICATION:	**MOS8**
		PACKAGE:	**9X10 PBGA**		
		LEAD COUNT:	**86 BUMP**	JOINT QUAL SPEC REV:	**T**

PURPOSE: **QUALIFICATION OF 86 BUMP PBGA**

PACKAGE RELIABILITY (Preconditioning Temperature Cycle (–65 to +150°C + bake (125°C, 24 hours) + (30°C, 60% RH 48 hours) + infrared reflow (230°C, 20 seconds, two passes)

Stress	Conditions	Results	Hours/Cycle	Next Readout	Pass/Fail
		Actual Data			
Preconditioning	As Above	0/225	2 Passes	Complete	P
Temperature Humidity Bias	85°C/85% RH/5 V	0/45	1008 Hours	Complete	P
Temperature Cycle	–65 to 150°C Air/Air	0/90	500 Cycles	Complete	P
Autoclave	121°C/100% RH 15 PSIG	0/90	96 Hours	Complete	P

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