APPLICATION NOTE

AN052

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As microprocessors, memories, logic and ASICs drive to both higher performance and densities via dramatically decreasing process geometries, 5 Volt system design is rapidly becoming impractical. Power dissipation alone has become a critical issue for the latest multi-million transistor microprocessors and it is unlikely that new high performance CPUs will be offered at 5 Volts.

Intel has already stated that future versions of **both** the 486 and Pentium will be 3.3 Volt products. Thus the focus for 3.3 Volt design is rapidly expanding to include both portable, low-power applications and high performance systems.

While numerous products have been announced in the PLD area that offer 3.3 Volt operation, thus far the emphasis has been on reducing power consumption for portable applications. Most often, these devices are 5 Volt products that have simply been re-characterized for operation at 3.3 Volts. Unfortunately, this approach typically involves several negative trade-offs including low speed operations, low output drive capability, and the inability to tolerate 5V I/Os. Given the emerging trend toward 3.3 Volt high performance CPUs and systems, designers will soon require high performance 3.3 Volt PLDs that are fully functional without these critical shortcomings.

Designers facing the transition to 3.3 Volts need to consider several important factors that will influence their system design. These factors can be broadly characterized as performance, mixed voltage system operation, ground/V_{CC} bounce, and graceful power control.

3.3 Volt High Performance

The inevitable march of clock rates to higher frequencies affects not only the design of high performance workstations and PCs, but also surrounding peripherals, communications equipment, and supporting embedded applications. Thus it is not sufficient to merely offer slow versions of 5 Volt products to satisfy the high performance requirements of 3.3 Volt system designers. These applications demand programmable logic that offers comparable performance to 5 Volt offerings. To accomplish this goal, PLD vendors need to develop both processes and designs that are specifically targeted at 3.3 Volt high performance. With BiCMOS, PLD vendors can take advantage of the bipolar transistor's ability to easily accommodate lower voltage operation without performance degradation.

When a CMOS design on a given level of technology is reduced from 5 Volt operation to 3.3 Volts, the "voltage in, current out" nature of the MOS transistor forces a reduction in the available output current from the device. This is because the gate input voltage swing is limited by the V_{CC} rails. This current can be recovered by increasing the size of the transistor, but a larger load is then presented to the preceding stage, resulting in a net performance loss. Thus, without resorting to a smaller process geometry and specifically smaller channel lengths and thinner gate oxides (which present new, exciting challenges to reliable programming), CMOS devices are limited to providing slower 3.3 Volt operation, or compromising on output drive capabilities to a severe degree.

BiCMOS designers on the same process rules have the inherent advantage of being able to use bipolar transistors in the speed path. The bipolar transistor is in practical terms a current gain device. Its driving base-emitter voltage is relatively constant, requiring only a few hundred millivolts to turn the output on or off. The required DC driving current is provided by simply sizing the input resistor. If the supply voltage is reduced from 5 to 3.3 Volts, this input resistor is simply reduced accordingly to provide the same current. As a result, since the current is the same, the reduced voltage reduces the DC power by approximately 34%. This approach works because the bipolar transistor does not know that the supply voltage is smaller. Its high performance switching speed is maintained, even without exotic process optimization for 3 Volts.

Future improvements in BiCMOS process technology will enhance performance even further. The primary drawback to bipolar transistors is that they suffer relative to CMOS in terms of circuit complexity. By utilizing BiCMOS, circuits that are in the critical path can utilize bipolar devices, and CMOS devices can be utilized for the control logic needed in programming and test circuitry. Thus BiCMOS gives circuit designers the ability to provide competitive high performance 3.3 Volt devices on proven, existing process technologies.

Mixed 3V / 5V Design

While 3.3 Volt systems are clearly the next emerging standard in system design, the momentum of the past will not disappear overnight. It is clear that some older design components will still remain exclusively available at 5 Volts. In these cases it is imperative that consideration be given to mixed 3.3 / 5 Volt systems. Fortunately, the logic thresholds for 3.3 Volts are the same as 5 Volt TTL: V_{IL} is 0.8V (max.), and V_{OH} is 2.0V (min.). Therefore, properly designed devices can greatly simplify interface requirements to/from 5 Volt system components. Examining the input and output requirements, the ability of a device to allow both input and output voltages that are higher than the 3.3 Volt V_{CC} is critical. 3.3 Volt devices that do not allow 5 Volt inputs are likely to fail when interfacing to 5 Volt CMOS devices that drive full rail outputs.

For 3.3 Volt devices driving 5 Volt logic, the ease with which both TTL and CMOS logic levels can be supported is a key consideration. Philips LVT devices provide an excellent case in point. LVT output drivers swing virtually between the power supply rails allowing direct interface to 5V TTL logic. Additionally, LVT outputs are designed to support the use of external pull-up resistors to 5 Volts. This provides the ability to force outputs on 3.3 Volt LVT devices to 5 Volts and thus provide a simple, direct interface to CMOS logic levels.

In the case of 5 Volt logic driving 3.3 Volt device inputs, it cannot be overstated that it is imperative that the input structure be capable of withstanding voltages that are higher than their V_{CC} voltage. Philips LVT devices have been designed specifically to accommodate input voltages as high as 7 Volts allowing direct interface to CMOS full-swing and Totem-pole outputs. In the case of 5 Volt open-drain outputs, a simple pull-up resistor would be required (which is the usual case with this output type). Reliable system operation may be severely compromised if a 3.3 V device allows current to "leak" into a pin that has a 5V overvoltage applied. Measuring this stray current is an important criteria that component engineers should examine when evaluating 3.3V devices.

For both inputs and outputs, properly designed 3.3 Volt devices can vastly simplify the task of mixed voltage system design. In the case of LVT PLDs, this provides logic and control functionality at the interface. This provides significantly more flexibility and control than level translators alone while transitioning to full 3.3 Volt systems.

Ground and V_{CC} Bounce

Another source of concern for high performance 3.3 Volt system designers should not be particularly surprising. Ground bounce continues to be an issue in high speed devices that have utilized output drivers sufficient to switch a 50pF load in less than 2nS. The unfortunate side effect is that these drivers, when switching from high to low, create an instantaneous current rush into the device.

This current rushes in faster than it can be dissipated through the ground pin(s), due to the inductance of the ground path. The observable result is that an output that should stay low while other drivers are switching will “bounce” high. Of concern to system designers is the bounce magnitude and duration. In a worst-case scenario, with a large number of outputs switching, and active low level output could bounce above the switching threshold between 0.8 and 2.0 Volts long enough to adversely affect system integrity. This is particularly true when a PLD is being used to generate a clock (for instance, in a FIFO application) or drive asynchronous logic.

Since ground bounce is directly proportional to package inductance, high speed designers have favored lower inductance surface mount packages such as PLCC and SOIC. Beyond simple changes in packaging preferences, most silicon vendors have incorporated controlled edge rates in their output structures as well. From a process perspective, ground bounce can be dramatically reduced by utilizing advanced BiCMOS processes. CMOS outputs suffer from inherent disadvantage because of the bi-directional nature of the MOS transistor.

A CMOS n-channel transistor capable of sinking a guaranteed 16mA of I_{OL} current is a device that when turned on, is equivalent to a 10Ω resistor between the output pin and ground. This couples any inductive spike appearing on the chip’s internal ground line directly onto the unswitched output pins.

By contrast, a BiCMOS device’s bipolar output transistor’s “on” resistance (also 10Ω) remains low only when current is flowing in one direction, from collector to emitter. If the current tries to flow in the opposite direction (in this case, from ground back into a static low output), the transistor immediately shuts off, breaking the path. This effectively damps the ground spike.

An indicator of the effectiveness of this approach is Philips 3.3 Volt LVT22V10-7. This device offers –16mA/32mA output drive capability, and with seven outputs switching, exhibits worst-case ground bounce of less than 0.8 Volts. It should be noted that the only competitive devices seen at this time offer very low output drive (–2mA/16mA) and exhibit typical ground bounce of 1.5V!

While ground bounce is not a new issue to high performance system designers, 3.3 Volt system design raises the possibility of V_{CC} bounce. Simply defined, V_{CC} bounce is the opposite of ground bounce. When simultaneous outputs make a low-to-high transition, an instantaneous current surge occurs. Once again, due to the inductive nature of the V_{CC} path, the current required lags demand. When this occurs, V_{CC} can drop, and active high outputs that should remain stable can glitch.

With 5 Volt systems, this was rarely a problem for system designers because of the wider 3 Volts of margin between V_{IH} of 2.0 Volts and 5 Volt V_{CC}. 3.3 Volt systems narrow this margin to just 1.3 Volts. As with ground bounce, the same rules and potential hazards apply. Designers should use low inductance packages whenever possible and request V_{CC} bounce data from vendors to ensure reliable systems.

Live Insertion / Dynamic Power Control

The advent of green PCs offering automatic power-down modes has increased consumer demand for products that use resources more intelligently. High performance 3.3 Volt products already offer lower power requirements than equivalent 5 Volt devices. But what about the ability to power down parts of your system during periods of inactivity? This system need, at a device level, requires that attention be paid to the operation of the input and outputs during power transitions. Specifically, device outputs that are not guaranteed to be in a high impedance state during power-up/down could cause reliability problems by inducing bus contention resulting in device failures.

Philips LVT family devices offer graceful power transition as well as live insertion capability via two distinct features. First, the I/O structures are free of both intentional and parasitic forward biased diodes or resistors between the pin and V_{CC} or ground. Second, the outputs are placed into a 3-State condition if V_{CC} falls within the threshold range of 0.8 to 2.0 Volts. This turns off both the pull-up and pull-down transistors of the totem-pole outputs during power-up/down until V_{CC} rises to an adequate level. These features give designers the freedom to configure systems for both dynamic power-down and live insertion capabilities.

With the major microprocessor, memory, and logic suppliers moving to 3.3 Volts, there remains no doubt that system designers will be confronted with demands for 3.3 Volt high performance systems. By paying attention to traditional high speed design considerations, the issues that accompany 3.3 Volt systems are relatively few. Devices clearly need to meet both current and future performance requirements. For the near term, devices that can easily accommodate mixed voltage design will greatly simplify the transition from 5 Volt to 3.3 Volt systems. Ground bounce considerations stay with us and are accompanied by the potential for V_{CC} bounce. Designers should be aware of both issues and ask their vendors for relevant data. Finally, while 3.3 Volt designs will by their nature offer power savings, choosing devices that are capable of providing power down during periods of inactivity will allow designers the ability to increase these savings. Philips LVT22V10 devices have been designed to address these important issues that will soon be facing system designers.

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